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First Record of Single Event Upset on the Ground, Cray-1 Computer Memory at Los Alamos in 1976

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Abstract:

Records of bit flips in the Cray-1 computer installed at Los Alamos in 1976 lead to an upset rate in the Cray-1's bipolar SRAMs that correlates with the SEUs being induced by the atmospheric neutrons.

I changed the numbers for the associations above so EN is 1); Boeing is 2); LANL is 3); Cray is 4).

In figure captions, do you want to use Figure 1 or Fig. 1? Both are used in the paper.

Do you want periods after the roman numerals for the different sections?

First Record of Single Event Upset on the Ground, Cray-1 Computer Memory at Los Alamos in 1976

I. Introduction

In 1976 the Cray Research Company delivered its first supercomputer, the Cray-1, installing it at Los Alamos National Laboratory. Los Alamos had competed with the Lawrence Livermore National Laboratory for the Cray-1 and won, reaching an agreement with Seymour Cray to install the machine for a period of six months for free, after which they could decide whether to buy, lease or return it [1]. As a result, Los Alamos personnel kept track of the computer reliability and performance and so we know that during those six months of operation, 152 memory parity errors were recorded [2]. The computer memory consisted of approximately 70,000 1K×1 bipolar ECL static RAMs, the Fairchild 10415 [3]. What the Los Alamos engineers didn't know is that those bit flips were the result of single event upsets (SEUs) caused by the atmospheric neutrons.

Thus, these 152 bit flips were the first recorded SEUs on the earth, and were observed 2 years before the SEUs in the Intel DRAMs that had been found by May and Woods in 1978 [4]. The upsets in the DRAMs were shown to have been caused by alpha particles from the chip packaging material. In this paper we will demonstrate that the Cray-1 bit flips, which were found through the use of parity bits in the Cray-1, were likely due to atmospheric neutrons. This paper will follow the same approach as that of the very first paper to demonstrate single event effects, which occurred in satellite flip-flop circuits in 1975 [5]. The main difference is that in [5] the four events that occurred over the course of 17 satellite years of operation were shown to be due to single event effects just a few years after those satellite anomalies were recorded. In the case of the Cray-1 bit flips, there has been a delay of more than 30 years between the occurrence of the bit flips and the identification of their cause as SEUs induced by the atmospheric neutrons.

II. Brief History of Cray Computer

Seymour Cray began working with computers in 1950, first for Engineering Research Associates (ERA) in St. Paul, MN, a company which changed ownership several times. In 1958 he joined Control Data Corporation (CDC) after it had been created by former employees of ERA. Seymour Cray was a key designer of the CDC 1604 which debuted in 1960 and of their next two even more successful computers, the CDC-6600 and CDC-7600. During the 1960s, Cray decided that he could accomplish a lot more if he were located away from the CDC headquarters in St. Paul, and so a new laboratory was set up for him in his home town of Chippewa Falls, WI which came to be known as the Chippewa Lab.

From 1968-72 he was working on the design of CDC's next computer, the CDC8600. By 1972 development of the 8600 hit so many roadblocks that Cray suggested to the CEO of CDC that a complete redesign was required, but CDC could not afford to do this for several reasons. As a result, Cray left CDC, creating a new company, the Cray Research Corporation, which he located immediately adjacent to the Chippewa Lab and also next to his home. However, the new laboratory was actually in the adjoining town of Hallie, and so it was known as the Hallie lab, where both the development and manufacturing were carried out, although he set up the business headquarters in Minneapolis. Cray brought over most of the technical team that he had assembled at CDC over the previous years.

In developing the brand new supercomputer design Cray introduced several innovations including the use of integrated circuits, ICs, rather than discrete components. Cray knew that the US military had been using ICs for almost a decade, as had the Apollo space program, so now, with the technology sufficiently matured, he chose to use ICs, which had the great advantage of drastically reducing the number of soldered interconnects. The ICs would also significantly

lower the power and heat consumption power consumption and heat production???. The original design would use only four different ICs, but very large quantities of them: 1) a 1K×1 bipolar ECL SRAM (in most cases the Fairchild 10415FC but comparable Motorola and Fujitsu SRAMs were also used), 2) a Fairchild 5/4 Logic NAND Gate, the SL56660, 3) a slower MECL 5/4 NAND gate and 4) a. Fairchild 'special' part, the SL82747.

Initially the new company had been financed by debenture bonds, but by 1975 Cray had a different idea, he wanted to take his small company public. Fortunately, even though some of the major computer manufacturers, IBM, Univac and Burroughs, were moving away from supercomputers, Seymour Cray had a national reputation as a computer design genius and many programmers around the country were admirers of his. Thus, when Cray's business manager flew to New York in early March 1976 to launch the public offering on Wall Street, within less than a week more than half a million shares were sold and $10 million was generated, which enabled the first Cray-1 to be completed.

The business manager next had to find a customer and he went to several of the national laboratories offering them the first machine of its kind. Engineers and scientists at both the Los Alamos and Livermore laboratories wanted to buy it, but the Energy Research and Development Administration (ERDA, predecessor agency to DOE) would purchase only one, and so each laboratory competed for the Cray, thereby preventing the other from being chosen. Cray himself broke the stalemate by offering Los Alamos the opportunity to keep the computer for 6 months on a trial basis, at no cost, allowing them to decide whether to buy, lease or return it afterwards. After the trial period Los Alamos publicly proclaimed that the Cray-1 was five times faster than the CDC7600 and signed a long term lease with Cray's company. Other customers followed suit, and Cray computers spread around the country. At Los Alamos, over the next two decades, the laboratory would install ___ different Cray computers.

III. Cray-1 Installed at LANL and its Bit Flips

A. Cray-1 Performance

The Cray-1 was installed on the first floor of Building 132 in Tech Area 3 of the Los Alamos National Laboratory. This part of Bldg 132 has only a basement and a first floor with a concrete roof and so the Cray-1 was shielded only by a concrete roof.

A total of 152 memory parity errors in the Fairchild 10415FC SRAM were recorded during the Cray-1 trial period in 1976 which lasted 25 weeks, from April 5 until Sept. 24. Even in 1976, in the design of the Cray-1 the Cray engineers recognized the need to include parity bits with each byte to signal that one of the bits has had? been changed for whatever reason.

B. Bit Upset Rate in Cray-1 in 1976

During the 25-week trial period in 1976, the Cray-1 averaged 5.2 hours/day of computer operation, thus the total number of hours the Cray-1 was run was 910 hours. The Cray-1 contained ~7.4 E4 of the 1K bit memory chips and was run in a mode that used the full 64 bit words for a total of 7.5E7 bits. As indicated, a total of 152 memory parity errors were recorded.

With the number of upsets, number of bits being used and the hours of we can calculate the bit upset rate. However, rather than calculate the rate directly, following [JESD89A], the SEU rate

data can be put into the form of an averaged SEU cross section, $\overline{\sigma_{SEU-bit}}$) that is due to the entire spectrum of the atmospheric neutrons, as shown in Eq. 1.

$$\overline{\sigma_{SEU-bit}} = N_{upset} / (\Phi_{spec} \times N_{bit}) \quad (1)$$

In this case, Φ_{spec} is the atmospheric neutron flux, E> 10 MeV, at Los Alamos. The neutron flux in Los Alamos is calculated to be 6 times larger than that in New York City [6] (For what it's worth, I've seen 6.4 used before, based on a Gordon and Goldhagen article), leading to a flux of 84 n/cm²hr [7]. Thus, the bit upset rate was 152 Up/(7.5E7 bit*910 hr) = 2.21E-9 Upset/bit-hr and this field error rate is converted to an effective SEU cross section for the Fairchild bipolar SRAM of 2.6 E-11 cm²/bit.

C. Analysis Approach

The main analysis approach is to compare the error rate derived from the field upset data with the calculated SEE rate. In [5] the calculated cosmic ray error rate was predicted based only on calculations, and was about a factor of 2 larger than the field upset rate. For the Cray-1, we have measured laboratory data on the SEU response of Fairchild bipolar SRAMs. Thus, we will use the field upset rate to obtain the derived SEU response from the field upsets and compare it with measured SEU cross sections in Fairchild bipolar SRAMs. In reality, as discussed above, the upset rate data is transformed into an averaged SEU cross section, and this SEU cross section will be the basis for comparison.

D. SEU Rate in Fairchild Bipolar SRAMs

The Fairchild 10415 was a very early bipolar ECL SRAM. A small number of the early bipolar SRAMs had been tested for SEU and almost all of these were TTL designs not ECL. These SRAMs include the 93L422, 93L425, 93422 and 93425 [8]. In addition, Ziegler and his IBM colleagues report on the SER from the field as well as proton SEU cross sections, measured in a number of different bipolar SRAMs that IBM tested during the period of 1978-87 [9, 10]. This data is summarized in Table 1 and the SER values have been converted to SEU cross sections to enable meaningful comparison. The SEU cross section values range between 1-8 E-11 cm²/bit, with an average value of 3.5E-11 cm²/bit. It is not known whether any of the bipolar devices listed were ECL, but most likely they were TTL.

Fig. 1 Seymour Cray and Cray-1 Computer

Table 1 SEU Cross Sections of Bipolar SRAMs Measured by IBM in Field

# bits	SER	SEU, cm^2/bit	Comments	Ref
4K	6E3†	2.8E-11	Msr'd , Boulder, CO ('87)	9
4K	2.7E4†	4.5E-11	Msr'd , Lead-ville, CO ('87)	9
2E2	N/A	2E-11*	Qcrit =200 fC ('78)	10
2E2	N/A	1.5E-11*	Qcrit =240 fC ('78)	10
1K	N/A	8E-11*	Qcrit =200 fC ('86)	10
4K	N/A	6E-11*	Qcrit =200 fC ('86)	10
4K	1.1E3†	2E-11	Based on NYC	10
9K	1E3†	0.8E-11	Based on NYC	10

† From field observations (atmospheric neutrons)
* Measured using 148 MeV proton

E. SEU in Fairchild 93L422 SRAM

Engineers at JPL tested the 93L422 (256×4) SRAM for susceptibility to SEU several times, going back to 1980, with both protons and heavy ions, and some of this data was published only in internal JPL reports. The two main sources of publicly available proton SEU data on the 93L422 that show the SEU cross section variation with proton energy are [8] and [11]. In [8] they distinguish between the 93L422 devices from Fairchild and AMD, and also have data on the very similar 93L425 (1K×1) SRAM. In [11] only one set of cross section data is presented that was obtained from JPL. The proton cross sections in the two papers are similar except at the two highest energies, 350 and 590 MeV. Ref [8] made the actual measurements, but it is likely that not all of the data taken by the author were published by him in [8]. Thus, it is possible that other measured data were taken by JPL and were made available to be included in [11], and as verification of this, in Ref [12], also by the author of [8], a notably lower value of the 590 MeV cross

section point is given. Thus, we have plotted the SEU cross sections from [8], [11] and [12] in Figure 2, which shows the measured values, a smooth Weibull fit and a piece-wise linear semi-log fit. The agreement in cross sections at lower proton energies (< 100 MeV) and disagreement at the higher energies is clearly seen.

In looking at the proton-measured SEU cross section data in Figure 2 it is clear that they do not follow a Weibull distribution very well at intermediate energies. Thus for purposes of obtaining a SEU cross section applicable to the atmospheric neutron spectrum, a better way to utilize the proton data is to use linear piece-wise fits (in semi-log space) to the cross section, weight this with the atmospheric neutron flux, integrate over E and then divide by total neutron fluence. When this was done with the fit to the Ref. [8] data, we obtain a weighted cross section of 8E-11 cm²/bit for the atmospheric neutron spectrum, and with the Ref. 11 data it is 4.7E-11 cm²/bit (note that this value is approximately the average cross section over the energy range of 50-600 MeV with the Ref. [11] data).

Thus, we estimate that the SEU cross section in the 93L422 due to the atmospheric neutron flux is in the range of ~5-8 E-11 cm²/bit. In [8] measured proton SEU cross sections for the very similar bipolar SRAM, 93L425, are given, and at the two highest energies, 350 and 590 MeV, the cross sections for the 93L425 are a factor of 2 lower compared to the 93L422, but at 160 MeV, the cross section is only a factor of 1.2 lower. This again points out some uncertainty in the proton SEU cross sections in Ref [8] but it is the only source of data that is available.

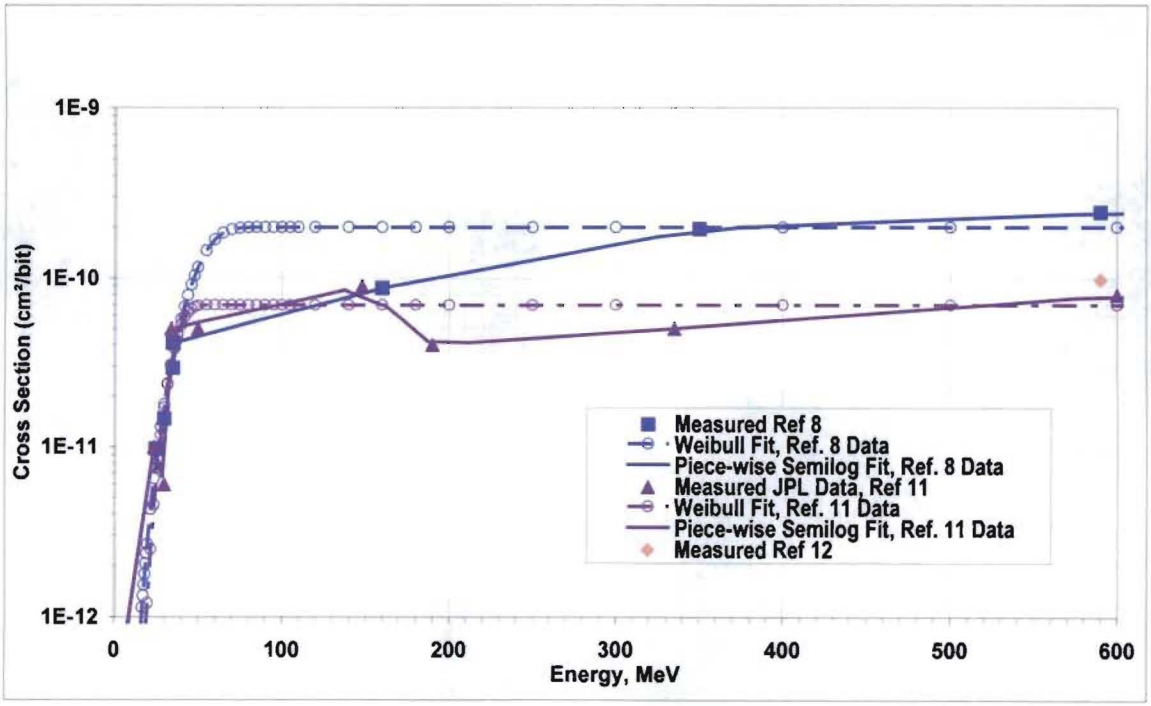

Figure 2 Comparison of Measured and Fitted Proton SEU Cross Sections in Bipolar 93L422

F. ECL/TTL SEU Sensitivity

The actual Fairchild bipolar SRAM used in the Cray-1, the 10415, is an ECL device whereas the 93L422 is a TTL device. Thus, we need to estimate the SEU sensitivity of a bipolar ECL SRAM compared to a bipolar TTL SRAM. Very few ECL parts have been tested for SEE because they were known to be very susceptible to SEU and also consume more power than TTL devices. The best data is in [13] in which 3 ECL SRAMs were tested, but none were from Fairchild. One of these, a Fujitsu 10474 appears to be somewhat similar to the Fairchild 10470 that was used in the Cray XMP. The proton SEU cross section for the Fujitsu 10474 (~3E-9 cm^2/dev or 7.5E-13 cm^2/bit at 55 MeV) is quite low compared to the SEU cross section for the 93L422.

A better approach is to compare the heavy ion SEU response of two different versions of the AMD 2901 4-bit slice processor, the 2901B which was a TTL device and the 2901C which was an ECL device. There are two sources of heavy ion SEU data for the 2901 B/C devices, tests by JPL [14] and Aerospace Corp. [15]. In the JPL data, SEU cross section vs. LET data [14], for the 2901B, the lowest LET point is at 6.4 MeV-cm^2/mg, but it is marked with a zero-response arrow indicating that SEUs were not seen at any lower LET. No such zero-response arrow is included in the 2901C data. Thus, in performing Weibull fits for the two devices, L0 for the ECL device is lower than it is for the TTL device. As a result, when applying the FOM method [16] to the Weibull fits, the FOM for the ECL device is higher than the FOM for the TTL by a factor of 2.5-3 indicating that the ECL device has a higher SEU sensitivity.

However, using the Aerospace data [15], and in particular, the composite SEU response cross sections, we obtain the opposite conclusion. For both sets of data, the heavy ion asymptotic cross section for the ECL part is higher than that for the TTL part, but with the Aerospace data, the LET threshold for the TTL part is lower than for the ECL part, while for the JPL data the opposite is true. The net result is that with the Aerospace data, the FOM for TTL part is higher than for the ECL part by a factor of ~1.3. Thus using the Aerospace 2901 B/C heavy ion SEU data, the ECL SEU response is lower than the TTL response by about a factor in the range of 0.4-0.8. However, with the JPL data the SEU response of ECL device is higher than that for the TTL device by a factor of ~ 2.5. Without any further clarification, we must conclude that the best approach would be to assume that the SEU response of TTL and ECL devices is about the same, i.e., the ratio is ~1.

G. SEE Testing of Fairchild ECL SRAM in 2010

Through a cooperative electronics distributor, we were able to obtain 30-year old samples of the Fairchild 10415 SRAM and perform SEU testing on them while exposed to neutron sources. Externally, these samples appear to be quite old, indicative of the data code of the samples, _____ which can be seen in Figure 3. The Cray-1 contained hundreds of memory boards each containing more than a hundred of these SRAMs. While we haven't been able to obtain a picture of a Cray-1 memory board, one of the gate array boards from the actual Cray-1 that operated in Los Alamos is shown in Figure 4.

A test board was designed to test the Fairchild 10415 SRAM, and also a related Fairchild SRAM, the 10470 (4K×1) that was used in the subsequent Cray computer, the Cray XMP. As ECL devices these SRAMs draw a lot more power than TTL devices and this had to be accounted for in the design of the test board.

[After Jerry Wert builds the test card and we test the 10415 SRAM, the SEU data will go here and will be included in Table 2]

PIN CONFIGURATION

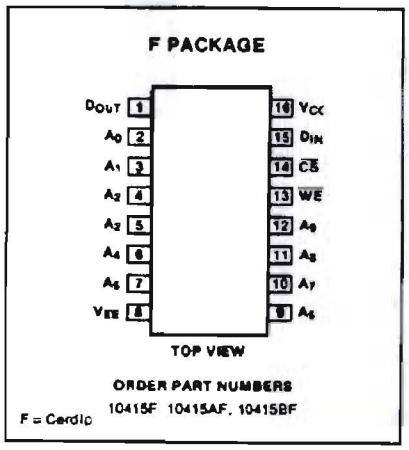

Fig. 3 (to be pic of actual 10415)

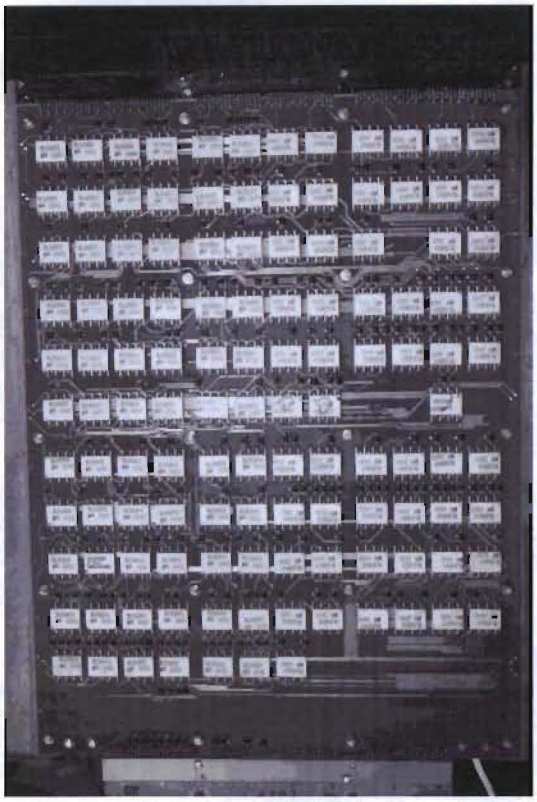

Figure 4 Board from LANL Cray-1 containing > 100 Fairchild SL56660 5/4 Logic NAND Gates

H. Comparison of Cray-1 Bit Flip Error Rate with Laboratory SEU Rate

Based on the Cray-1 bit flips during 1976, the effective SEU cross section for the Fairchild 10415 bipolar SRAM, derived from the field error rate, is 2.6 E-11 cm²/bit. Measured SEU cross sections in bipolar SRAMs from that same era shown in Table 1 are similar. An overall average of the SEU cross sections measured by IBM in at least four different bipolar SRAMs is 3.5E-11 cm²/bit. Using proton SEU cross sections measured in the Fairchild 93L422, the cross section due to atmospheric neutrons is in the range of ~5-8 E-11 cm²/bit. Based on the fewer measurements in the Fairchild 93L425 SRAM, the SEU cross section for an atmospheric neutron spectrum would be ~3-6 E-11 cm²/bit.

All of this data is summarized in Table 2. As seen in Table 2 there is excellent agreement between the SEU cross sections derived from the Cray-1 upsets and the measured proton SEU cross sections; that they are within a factor of 2 serves to corroborate the idea that the Cray-1 bit flips were due to SEUs in the 10415 SRAMs.

Table 2 Comparison of SEU Cross Sections in Cray-1 computer from Different Sources

Source	SRAM	Derived SEU X-Section, cm^2/bit	Assumptions
Actual parity errors in Cray-1 at LANL, 1976	Fairchild 10415 bipolar SRAM	2.6 E-11	Derived from rates for BTAG parity errors, CPU failures
14 MeV test, pro-rated, to atmospheric neutron environment, 2010	Fairchild 10415 bipolar SRAM		Ratio 2010 test (14 MeV neutrons) for 10415, 93L422 and 93L422 (row 4)
Testing by IBM 1978-1987	Diverse bipolar SRAMs	1-8 E-11	See Table 1
Measured monoenergetic proton SEU cross sections from SEU tests, 1980-1984	Fairchild 93L422	5-8 E-11	Proton SEU cross section function of E, integrated over atmosmospheric neutron spectrum

IV. SEUs in the ASC Q Supercomputer at LANL

A. Role of LANL regarding SEU by Atmospheric Neutrons

Since the Cray-1 was installed at LANL in 1976 and experienced its first SEU errors, LANL has become a key player in the work supporting the understanding of single event effects induced by atmospheric neutrons in microelectronics. Initially, during the 1990s, this centered around use of the WNR (Weapons Neutron Research) facility to simulate the atmospheric neutron environment. Since the 30 Left neutron beam provides the best match to the atmospheric neutron spectrum, this was the beam that was almost exclusively used to conduct SEE testing.

Various groups brought their test cards containing diverse electronics devices to the WNR to be placed in front of the 30-Left beam and various SEE effects (Is it redundant to write SEE effects?) were recorded: SEU, MCU (multiple cell upset), SEL (single event latchup), SEFI (single event functional interrupt) and SEB (single event burnout). Some of the data were published in NSREC papers, but much of it was considered proprietary by the groups that carried out the testing and paid for the beam time.

As the demand for beam time increased, the 30-Left facility was upgraded and modernized, making the SEE testing much more convenient to carry out. In its refurbished format it is called the ICE (Irradiation of Chips and Electronics) House. Thus, the LANL high energy neutron beam has been used for SEE testing primarily by outside customers from different industries: avionics, microelectronics, and computer server systems, etc. At present the demand for beam time exceeds its availability since

the entire Los Alamos Neutron Science Center (LANSCE) facility, of which it is a part, operates for less than 9 months per year, so alternatives are being considered.

B. Upsets Caused in LANL Computers

While all of the SEE testing was being conducted, there was anecdotal evidence of SEUs occurring and interfering with the operation of LANL equipment [Waters – this reference isn't in the reference list]. Further, the Advanced Simulation and Computing (ASC) Q supercomputer was deployed to Los Alamos in 2002, and it encountered more single-node failures than were predicted. After some investigation, the increased rate was hypothesized to be caused by SEUs in the BTAG SRAMs in Q's ES 45 Alphaserver nodes [17]. The BTAG SRAMs were protected by a parity check, but not ECC, so parity errors caused a node crash.

The ASC Q was located on the first floor of Building 2327 in Tech Area 3 of the LANL complex, the same Tech Area where the Cray-1 had been located 25 years earlier. This part of Building 2327 has only a basement and a metal roof above the first floor, so the Q supercomputer had only a metal roof over it affording essentially no shielding against the atmospheric neutrons.

Because single node failures in the operation of the Q supercomputer could increase the duration of large calculations, there was a strong interest within the ASC program to determine whether SEUs caused by cosmic ray neutrons were the primary cause of the elevated rate of single-node failures.

C. Testing and Analysis of SEUs in the ASC Q Supercomputer

As a result, an experiment involving hardware identical to that in Q's 2048 nodes was conducted during two separate time periods during 2002/2003. The ES45, which can contain up to four CPU boards, was exposed to the ICE House neutron beam. The chassis housing the hardware under test was positioned to allow various components and boards to be exposed during each test run, and more than 200 individual test runs were made. Extensive analyses were performed comparing errors observed in Q to the relevant data from the ICE House testing [17]. The tests considered for the analyses presented here involve one of two test programs, Memtest or Btagexer; see [17] for more details of the experimental procedure.

Compared to the situation with the Cray-1, the ASC Q supercomputer provides a great deal more and SEU-specific related data. With this data [Sarah, Harris], we can perform an analysis similar to what was done in Section III on the Cray-1 upsets. Table 3 contains the SEU cross sections derived from both the operation of the ASC Q supercomputer and the testing conducted at the ICE House.

Table 3 SEU Cross Sections for ASC Q Supercomputer

Data Source	Errors/wk in Q (8192 BTAG SRAMs)	Derived SEU X-Section, cm^2/bit	Assumptions
Observed Average Weekly # of BTAG Parity Errors in Q (9/5/04 – 10/23/04)	24	6.9E-14	All these errors are due to SEU
Observed Average Weekly # of CPU Failures in Q (9/5/04 – 10/23/04)	27.7	8E-14	All these errors are due to SEU
ICE House Testing, Memtest Count Data	Avg= 17.4*	5E-14	Definitely due to SEU
ICE House Testing, Btagexer Count Data	Avg= 22.6*	6.5E-14	Definitely due to SEU

* Based on a statistical model described in [17]

For the Q supercomputer we were not able to learn which specific BTAG SRAM was used, only that it is a 150 nm technology device containing 18 Mbits of memory [what source should be cited for this info about the BTAG SRAM?]. However, with this information and some of the SRAM SEU trend data that has been documented [Slayman – I don't find this reference in the reference list] we can bound the SEU cross section for such an SRAM based on the testing of same technology SRAMs. Thus, we have three separate sets of SEU upset data: 1) the error frequencies observed in Q, 2) the results of the testing at the ICE House, and 3) the bounds on the SEU cross section (exposed to atmospheric neutrons) for a 150 nm SRAM, the same kind of SRAM used in the Q computer. Data taken from [S] was used to derive the SEU cross section per bit values for the same technology SRAM as was used in the Q supercomputer. This allows a comparison of the SEU cross sections from 1) Q's observed performance, 2) the ICE House test results and 3) SEU cross sections in a collection of 150 nm SRAMs exposed to atmospheric neutrons as tested by their SRAM manufacturers. All of these SEU cross sections are summarized in Table 4.

Table 4 Comparison of SEU Cross Sections in Q Supercomputer from Different Sources

Source	SRAM	Derived SEU X-Section, cm^2/bit	Assumptions
Observed Weekly Error Rate in Q (9/5/04 – 10/23/04)	HP chosen SRAM, 150 nm, 18Mb	6.9-8 E-14	Derived from rates for BTAG parity errors, CPU failures
Ice House Testing (2002 - 2003)	HP chosen SRAM, 150 nm, 18Mb	5-6.5 E-14	Derived from Memtest count data and Btagexer count data
Testing by SRAM Vendors (150 nm	150 nm SRAMs,	0.7-3.6 E-14	Based on data [S] various SRAM

devs) ~2000-2005	diverse vendors		vendors

Overall, these results are similar to those of the Cray-1 and the bipolar SRAMs it used as tabulated in Table 2. In both Tables 2 and 4 we have results from: 1) upsets during actual computer operation, 2) upsets from testing the actual SRAM used in the computer with a neutron (or high energy proton) source and 3) results from other groups who tested the same technology SRAMs in ICE House-like neutron beams and obtained similar SEU cross sections.

V. Conclusions

Acknowledgments

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