CRAY T3D™ MC Systems PE Configurations (S/N 6001 – 6015)

HMM-089-0

Cray Research Proprietary

Cray Research, Inc.

Record of Revision

REVISION	DESCRIPTION
	May 1994. Original printing.

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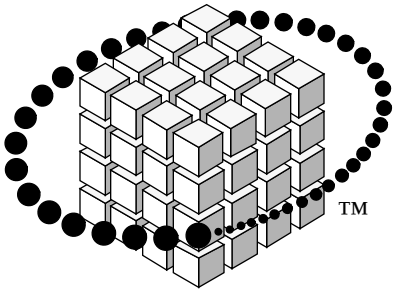


CRAY T3D MC Systems PE Configurations (S/N 6001 – 6015)

1 Document Overview

This document describes the hardware configuration characteristics that affect interconnect network routing, processing element node partitions, and barrier synchronization for each of the CRAY T3D multiple-cabinet (MC) systems with serial numbers 6001 through 6015.

The information provided in this document describes the communication links, module layout, and barrier synchronization circuits for each of the CRAY T3D MC systems.

1.1 Communication Links

For each system, a Y-dimension communication link figure is shown first, followed by figures that show the X- and Z-dimension communication links. Figure 1 shows a sample figure of the Y-dimension communication links.

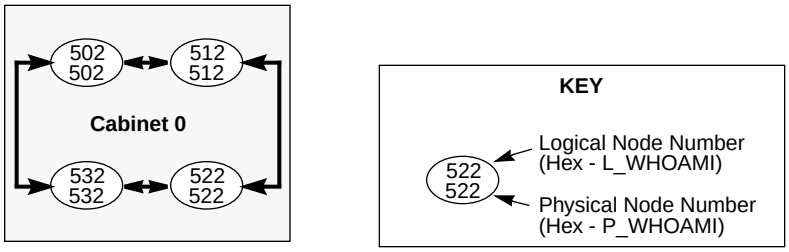


Figure 1. Sample Y-dimension Communication Links

In each of the Y-dimension communication link figures, the nodes (represented by the oval shape) contain two numbers. The top number shows the logical node number; and the bottom number shows the physical node number.

The logical node number is equivalent to the number read from a logical PE number (L_WHOAMI) register with bit 2^0 set to 0. For example, logical node 522_{16} contains the logical PEs 522_{16} and 523_{16}.

The physical node number is equivalent to the number read from a physical PE number (P_WHOAMI) register with bit 2^0 set to 0. For example, physical node 522_{16} contains the physical PEs 522_{16} and 523_{16}.

Figure 2 shows a sample figure of the X- and Z-dimension communication links. Each of the X- and Z-dimension communication link figures follows the same numbering convention as described for the Y-dimension communication links.

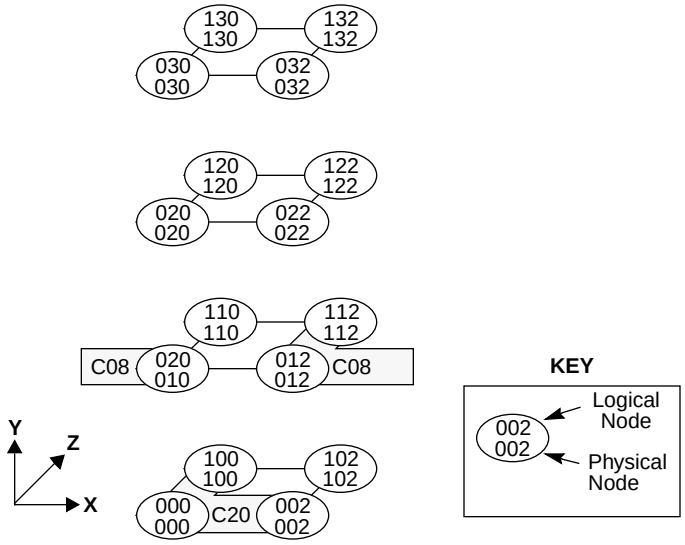


Figure 2. Sample X- and Z-dimension Communication Links

For clarity, the figures do not include the arrow heads on the communication links or the communication links that complete the torus in the X- and Z-dimension. Figure 3 shows how the torus communication links are connected in the Y=3 plane of nodes shown in Figure 2.

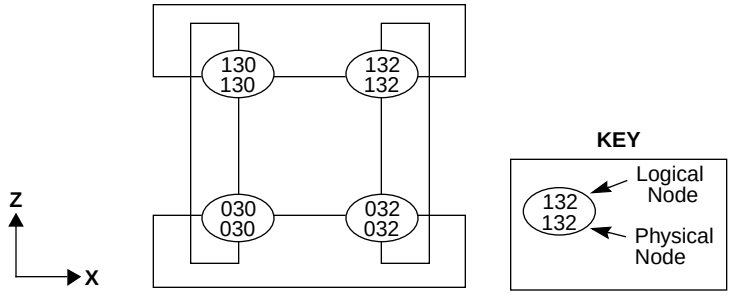


Figure 3. Sample Torus Communication Links

To keep the X- and Z-dimension communication link figures to a reasonable size, the exact positions of the I/O gateway nodes and spare processing element (PE) nodes are not shown. Instead, when a communication link between two PE nodes also connects to an I/O gateway or spare PE node, the communication link is highlighted and labeled with the physical node number of the I/O gateway input node or the physical node number of the spare PE node.

Figure 4 shows sample I/O gateway communication links. The most significant digit of the physical node number for an I/O gateway node is always C_{16}.

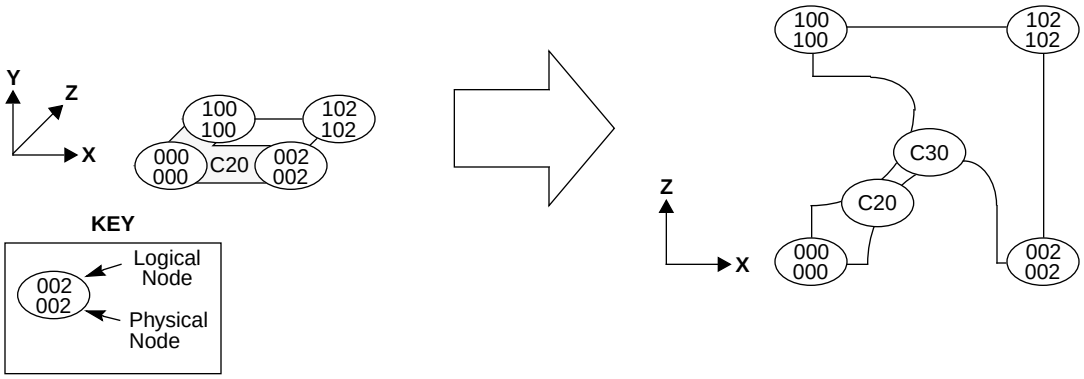


Figure 4. Sample I/O Gateway Communication Links

Figure 5 shows sample spare PE node communication links. The most significant digit of the physical node number for a spare PE node is always 9.

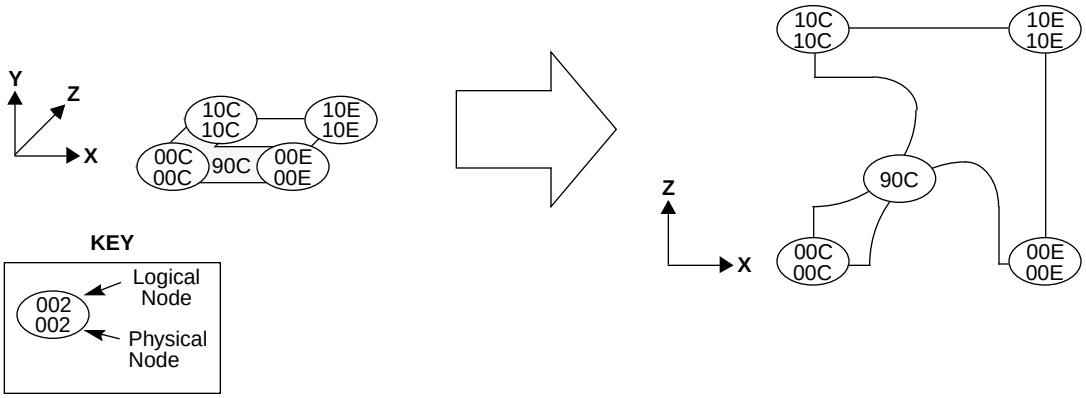


Figure 5. Spare PE Node Communication Links

Figure 6 shows sample communication links for PE nodes that connect to both I/O gateway nodes and a spare PE node.

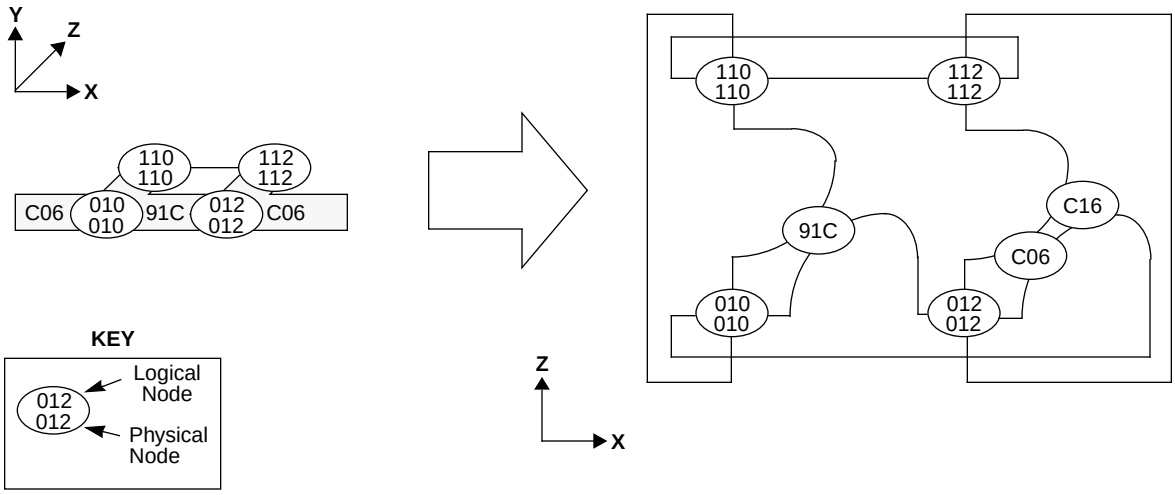


Figure 6. Sample Spare PE Node and I/O Gateway Communication Links

1.2 Module Layout

The module layout figures show the slot number a module resides in and show the physical nodes that are located on the module (refer to Figure 7). The physical node number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $61C_{16}$ contains the physical PEs $61C_{16}$ and $61D_{16}$.

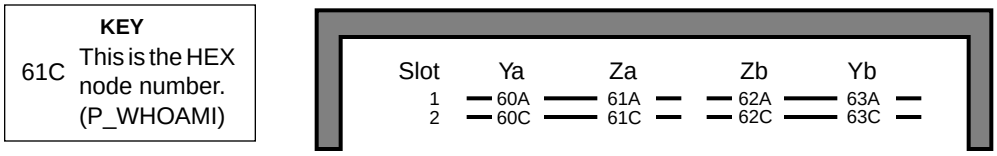


Figure 7. Sample Module Layout

1.3 Barrier Synchronization Circuits

The barrier synchronization circuit figures show the bypass point connections for each of the CRAY T3D MC systems.

2 CRAY T3D MC2048 System

The CRAY T3D MC2048 system contains 2,048 PEs in 1,024 processing element nodes and is housed in four cabinets. The following subsections describe the communication links, module layout, and barrier synchronization bypass points for the CRAY T3D MC2048 system.

NOTE: Throughout this document, physical PE numbers are represented as three-digit hexadecimal numbers that correspond to the physical PE numbers in the P_WHOAMI registers. For example, a PE may have a physical PE number of $10B_{16}$.

NOTE: Throughout this document, physical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $10A_{16}$ contains the physical PEs $10A_{16}$ and $10B_{16}$.

NOTE: Throughout this document, logical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a L_WHOAMI register with bit 2^0 set to 0. For example, logical node $10A_{16}$ contains the logical PEs $10A_{16}$ and $10B_{16}$.

2.1 CRAY T3D MC2048 Communication Links

Figure 8 shows the physical communication links between nodes in the Y dimension. Note that the nodes are not connected in sequential order of physical node number.

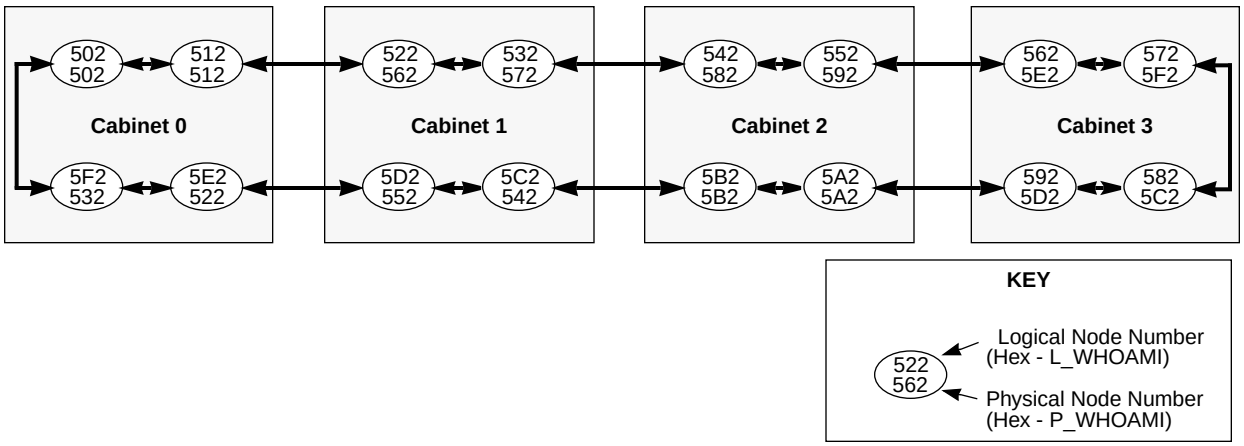


Figure 8. CRAY T3D MC2048 Y-dimension Communication Links

Figure 9 shows the physical communication links between spare nodes in the Y dimension.

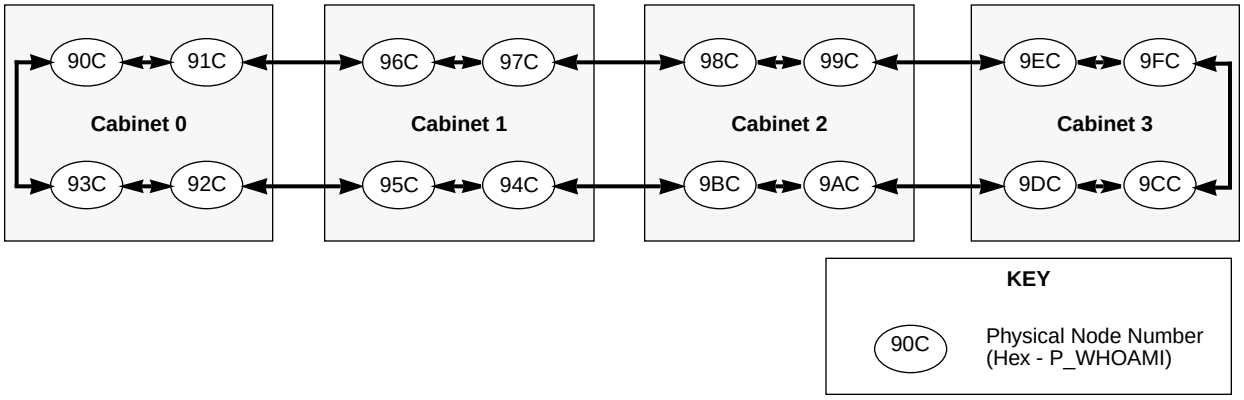


Figure 9. CRAY T3D MC2048 Spare Node Y-dimension Communication Links

Figure 10 through Figure 13 show the physical communication links between the nodes in the X and Z dimensions. For clarity, the figures do not show the communication links that complete the torus in the X and Z dimensions are not shown.

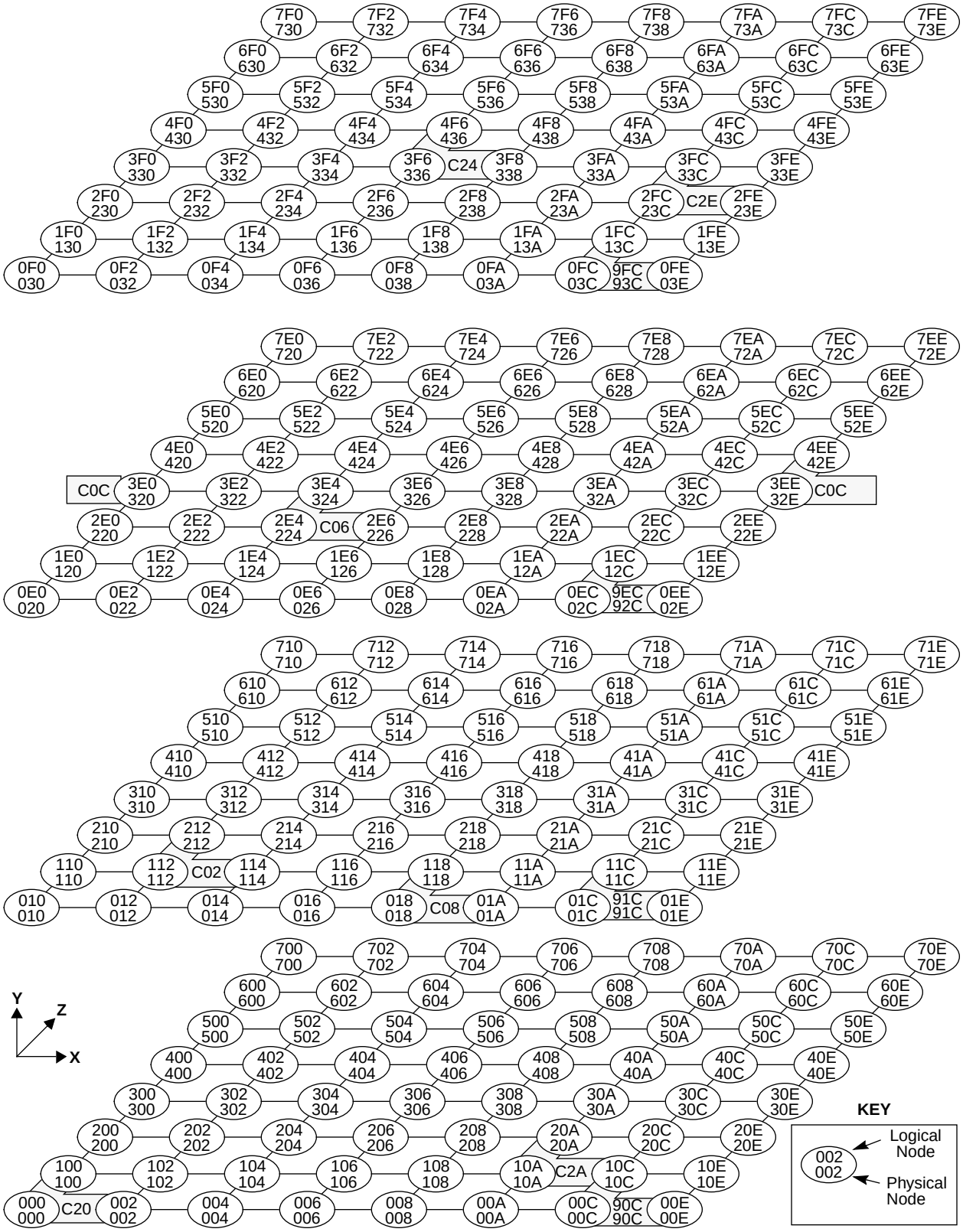


Figure 10. CRAY T3D MC2048 Cabinet 0 X- and Z-dimension Communication Links

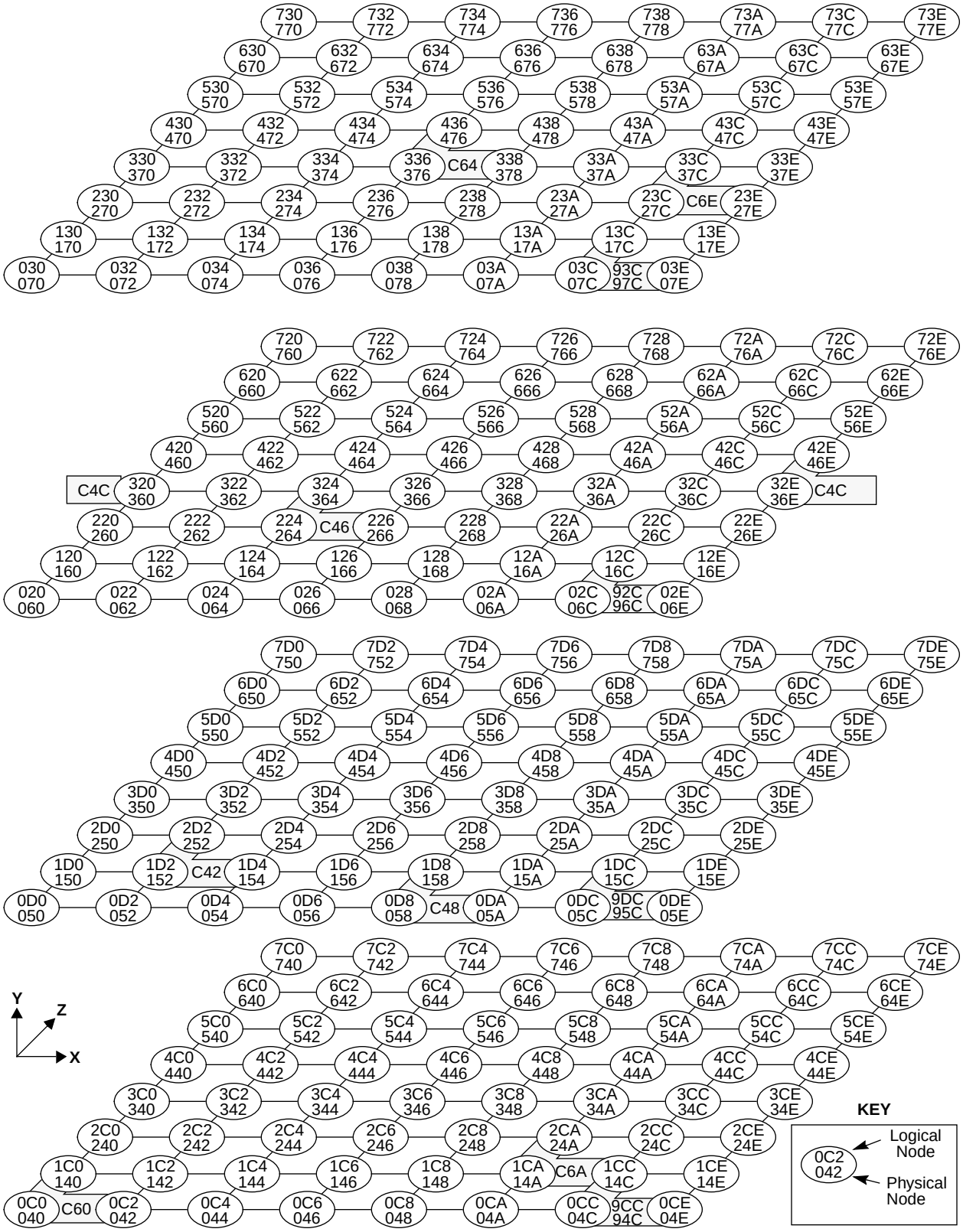


Figure 11. CRAY T3D MC2048 Cabinet 1 X- and Z-dimension Communication Links

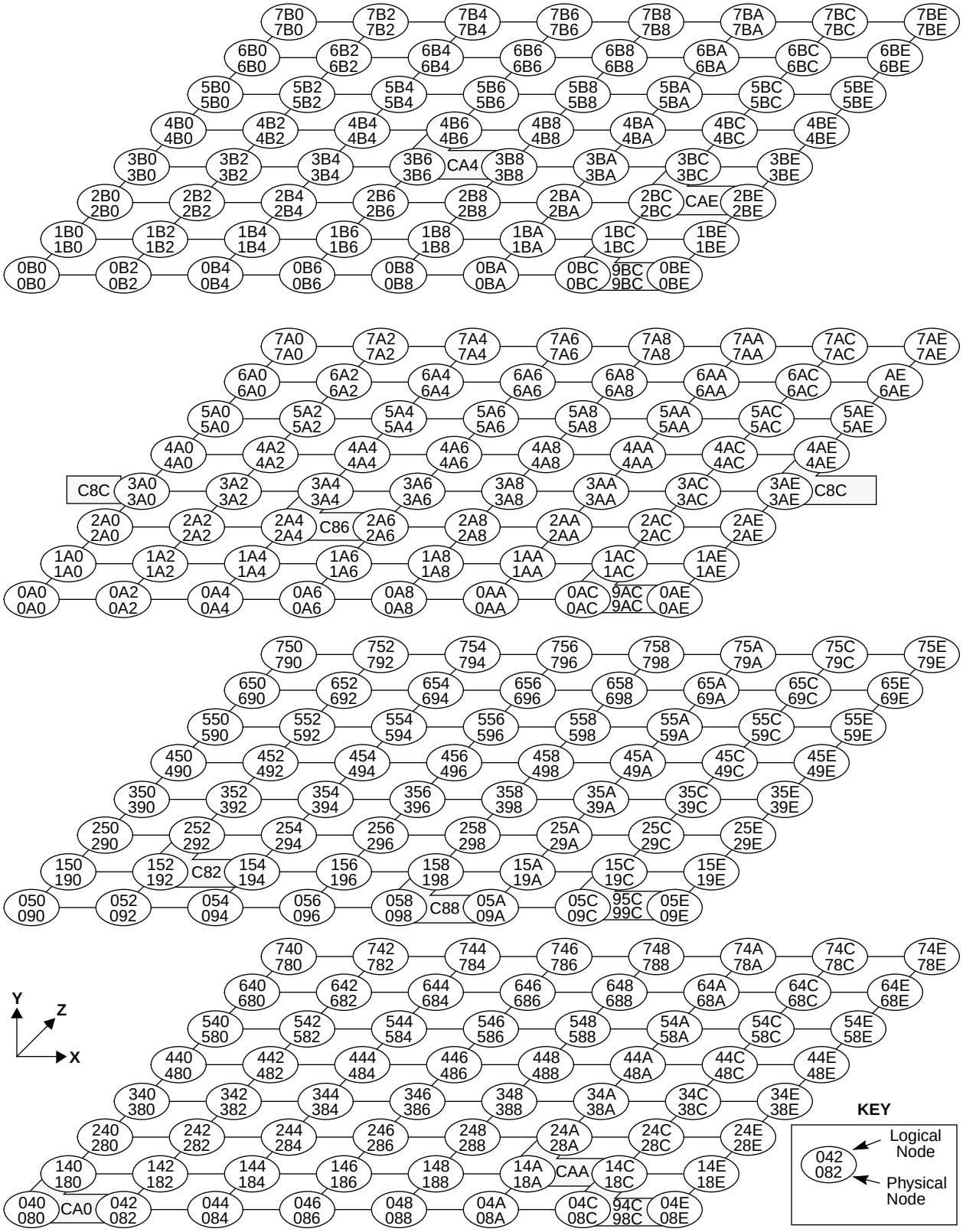


Figure 12. CRAY T3D MC2048 Cabinet 2 X- and Z-dimension Communication Links

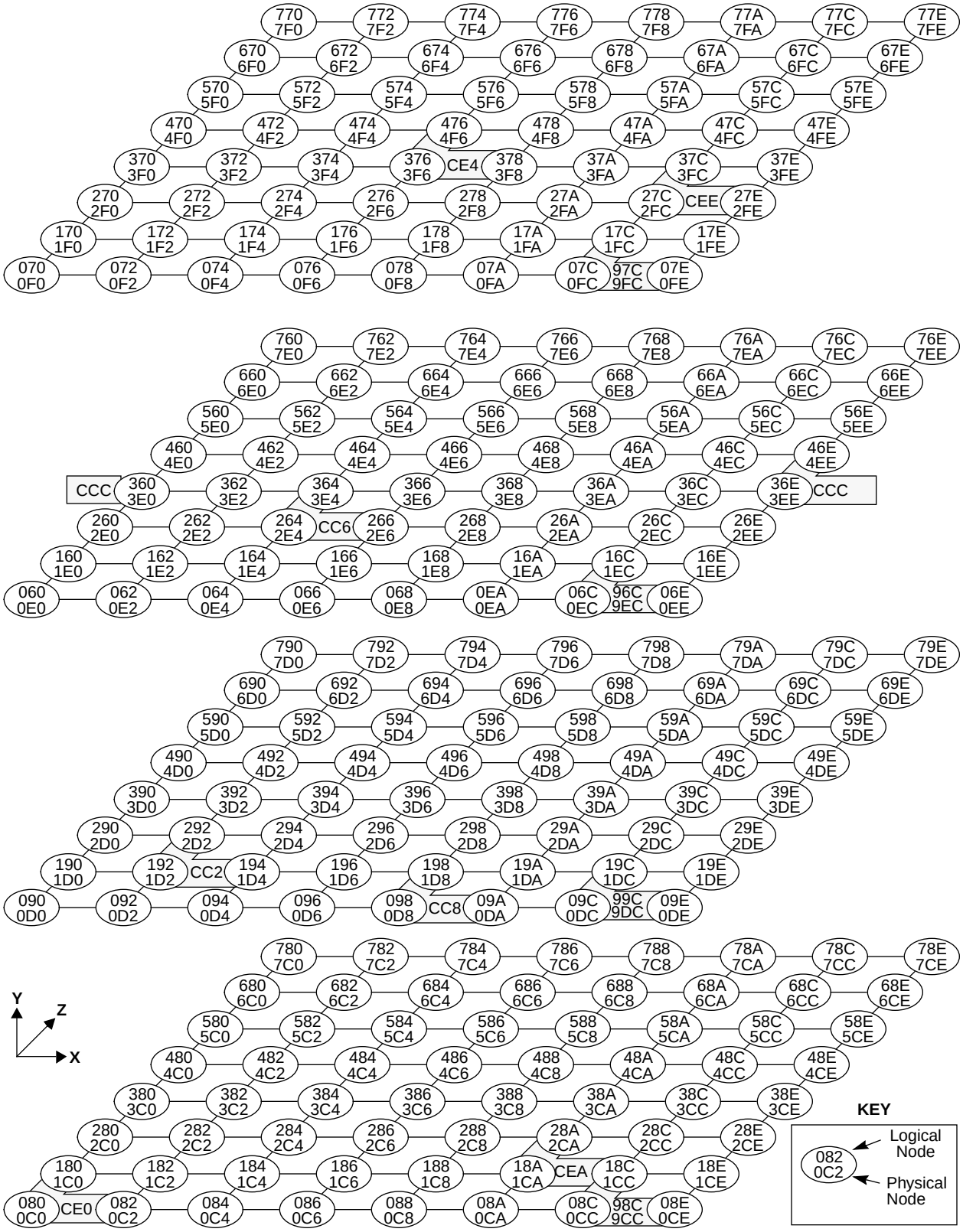


Figure 13. CRAY T3D MC2048 Cabinet 3 X- and Z-dimension Communication Links

2.2 CRAY T3D MC2048 Module Layout

Figure 14 through Figure 17 show the module layout and physical node locations in each of the four CRAY T3D MC2048 system cabinets. Each figure represents the physical node number as a three-digit hexadecimal number that is equivalent to the number read from the P_WHOAMI register with bit 2^0 set to 0. For example, physical node 002_{16} contains the physical PEs 002_{16} and 003_{16}.

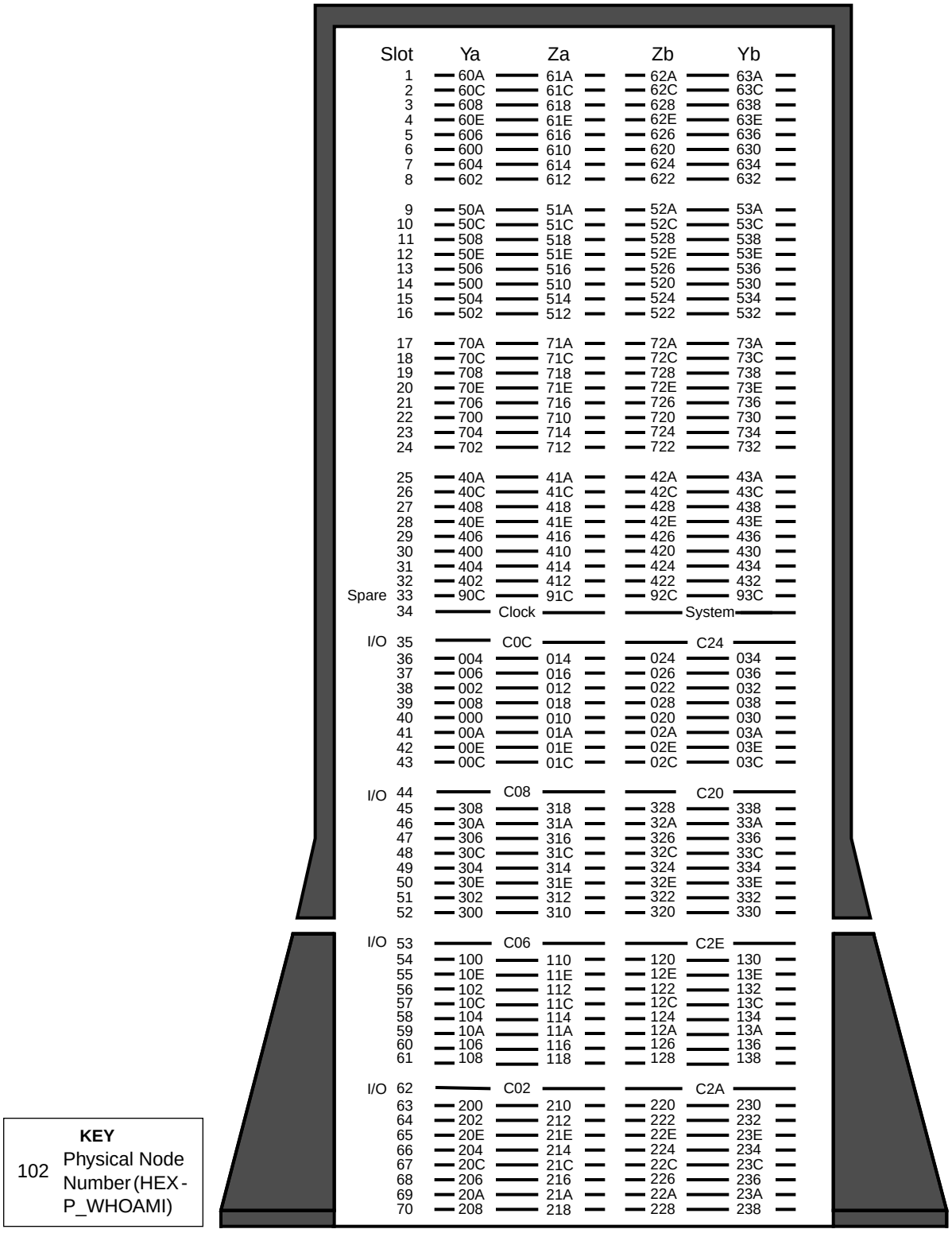


Figure 14. CRAY T3D MC2048 Cabinet 0 Module Layout

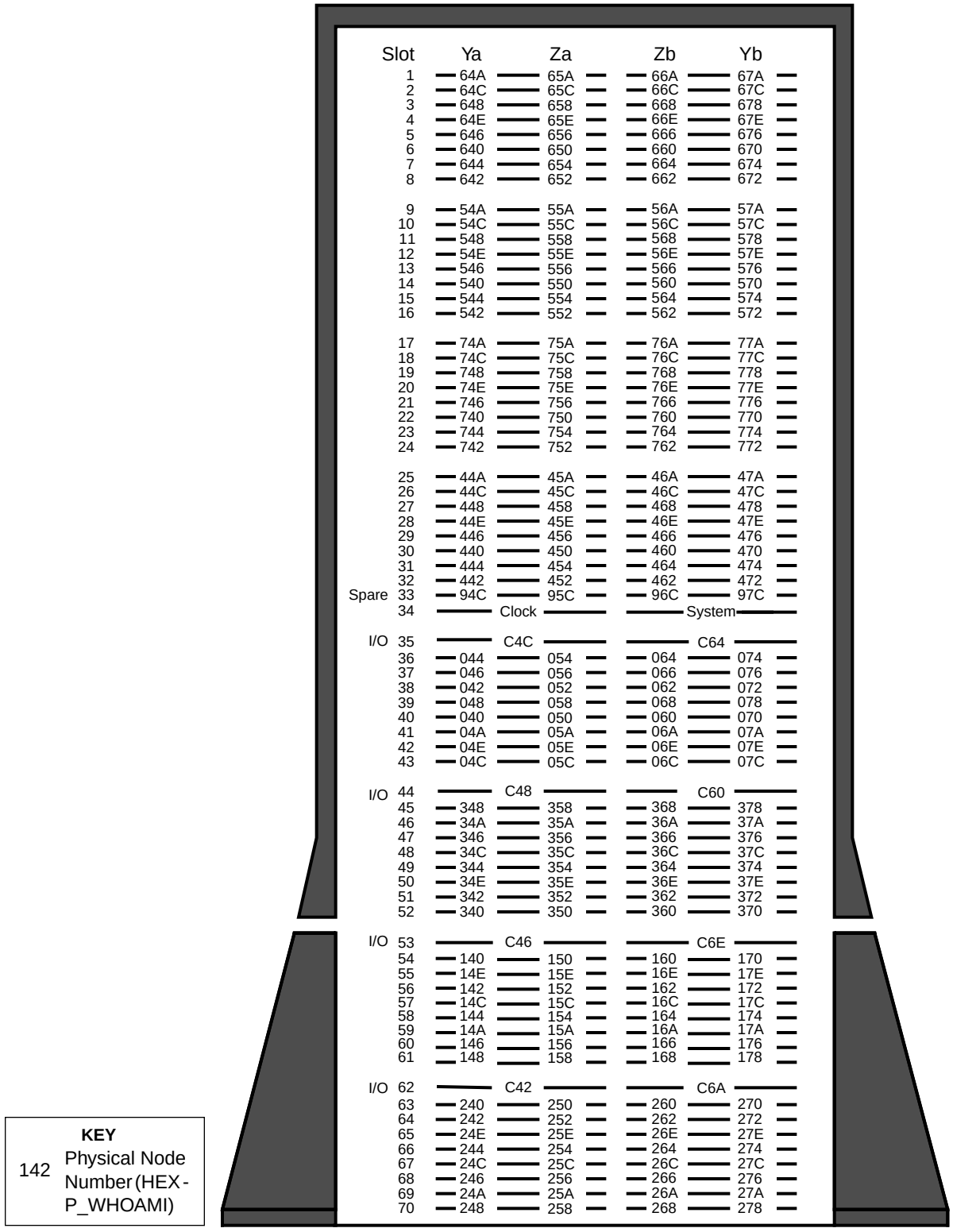


Figure 15. CRAY T3D MC2048 Cabinet 1 Module Layout

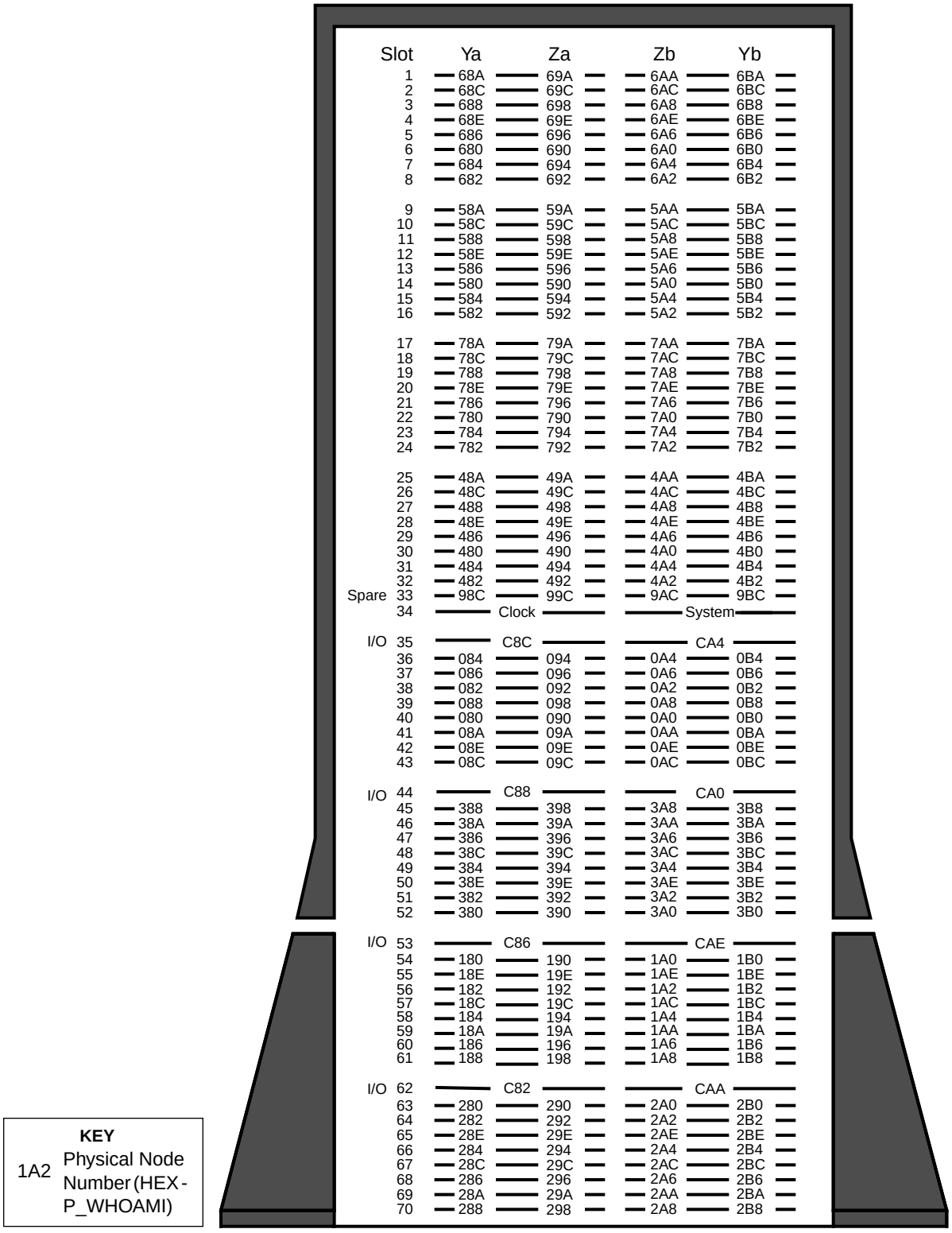


Figure 16. CRAY T3D MC2048 Cabinet 2 Module Layout

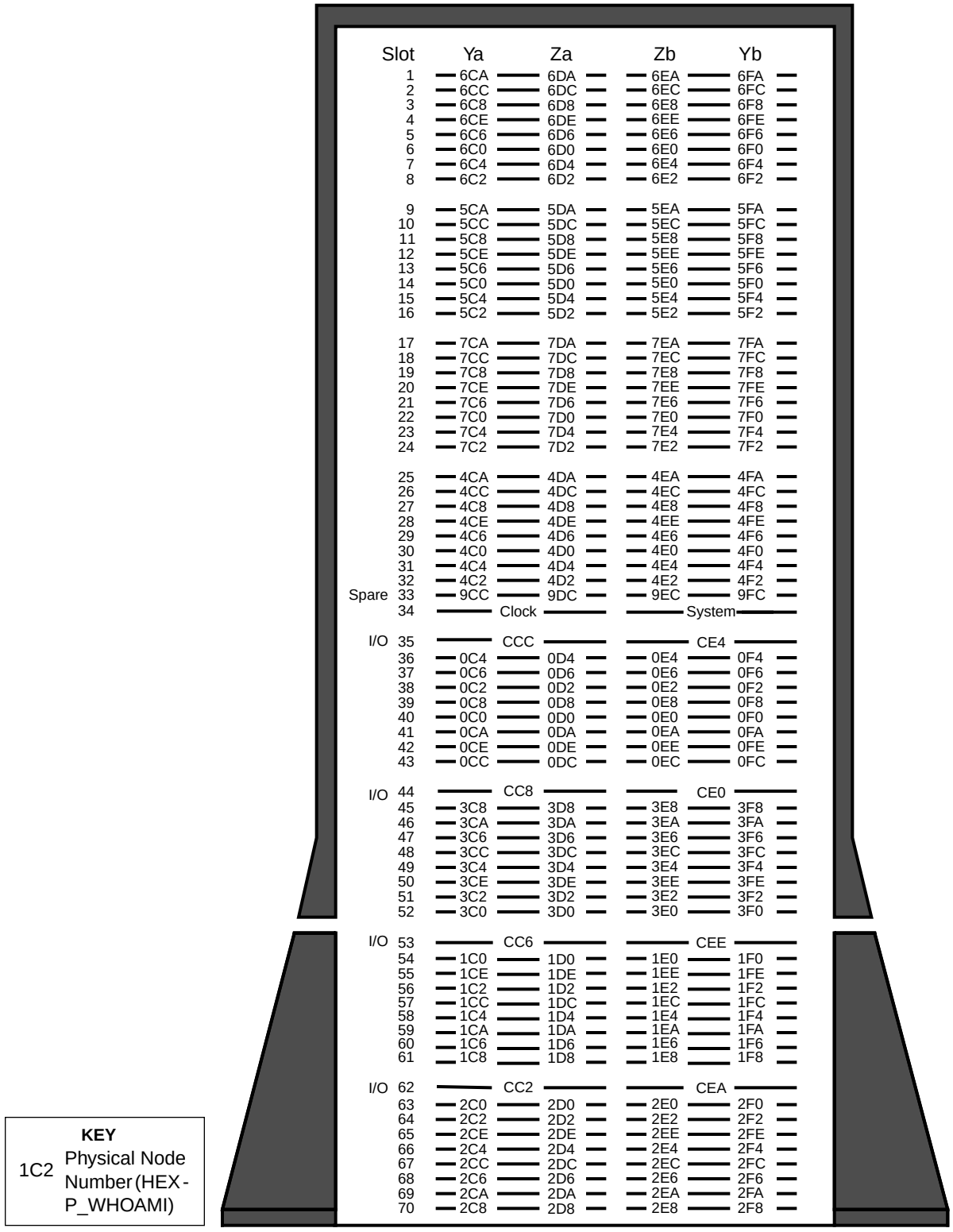


Figure 17. CRAY T3D MC2048 Cabinet 3 Module Layout

2.3 CRAY T3D MC2048 Barrier Synchronization Circuits

Figure 18 through Figure 37 show the barrier synchronization bypass points for all four physical barrier synchronization circuits in each of the four CRAY T3D MC2048 system cabinets. In these figures, the printed circuit board (PCB) bypass points and all other bypass points are shown.

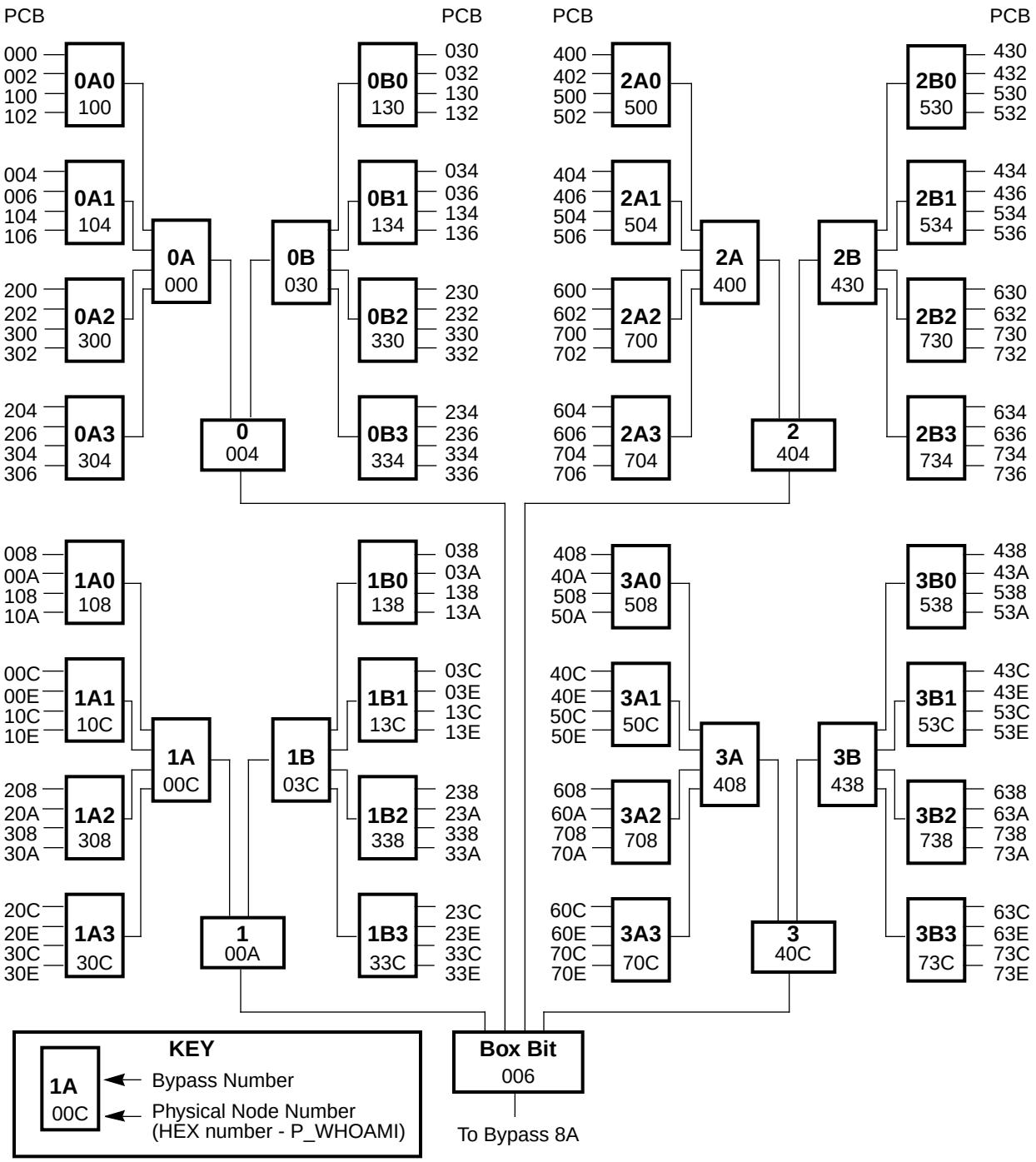
The PCB bypass points are controlled by bit 2^{11} or bit 2^{12} of the network mode register (NODE_CSR). Every processing element node PCB contains four PCB bypass points (one for each physical barrier synchronization circuit).

Each PCB bypass point is given a name that corresponds to the physical node that controls the bypass point. For example, the PCB bypass point 402 in barrier synchronization circuit 0 is located on the PCB that contains physical PEs 402_{16}, 403_{16}, 412_{16}, and 413_{16}. This bypass is controlled by setting bit 2^{11} of the NODE_CSR in physical node 402 (which contains physical PEs 402_{16} and 403_{16}) to the appropriate value.

When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 0, the output of the AND gate in a PCB bypass point is redirected to the fanout block in the bypass point. When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 1, the output of the AND gate in a PCB bypass point is directed to a second-level bypass point.

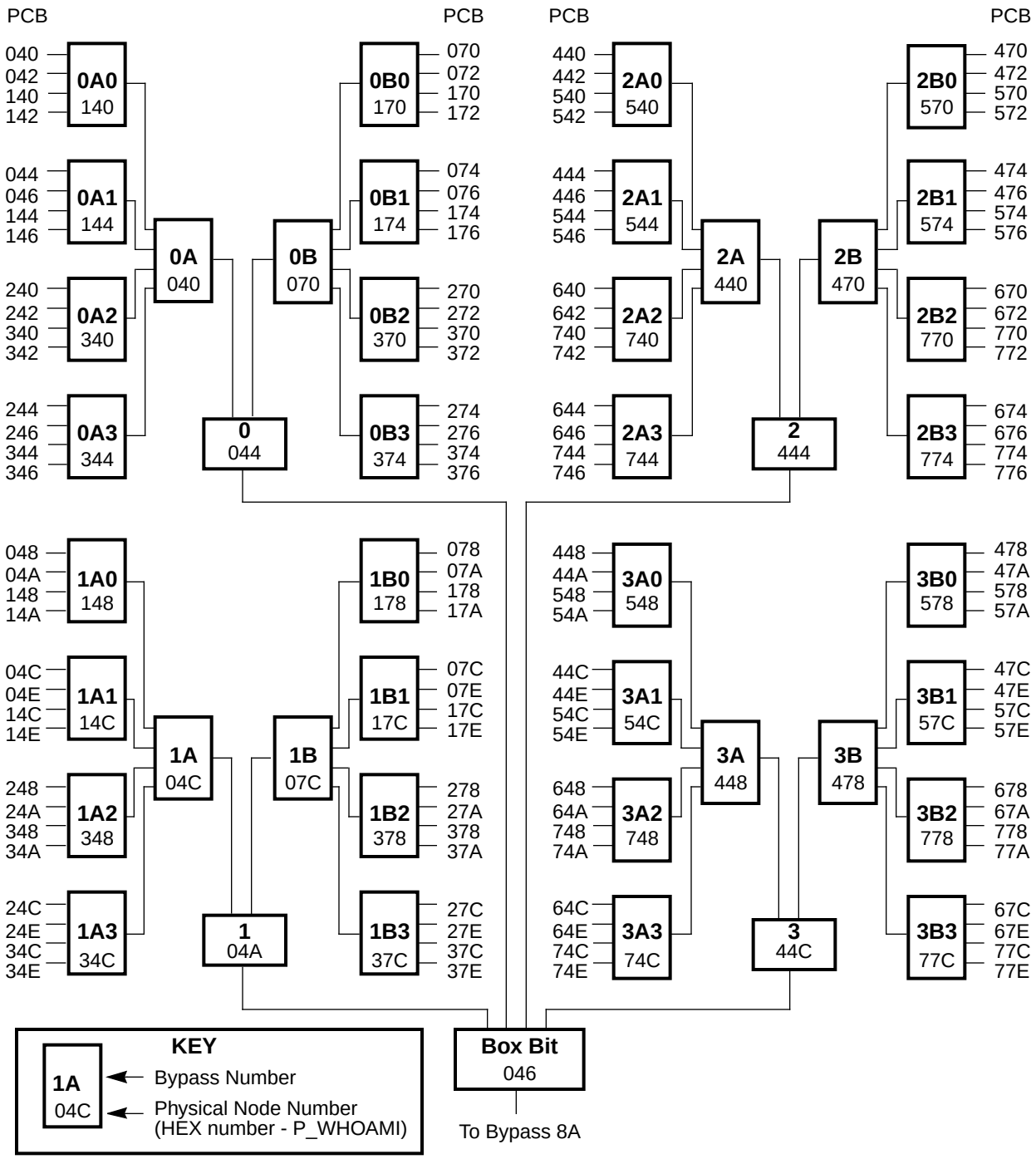
The other bypass points shown in the following figures are controlled by bit 2^{13} of the NODE_CSR. For example, bypass point 0A in barrier synchronization circuit 0 of cabinet 0 is controlled by setting bit 2^{13} of the NODE_CSR in physical node 000_{16} (which contains physical PEs 000_{16} and 001_{16}) to the appropriate value.

When bit 2^{13} of the NODE_CSR is set to 0, the output of the AND gate in the bypass point is redirected to the fanout block in the bypass point. When bit 2^{13} of the NODE_CSR is set to 1, the output of the AND gate in the bypass point is directed to the next-level bypass point.



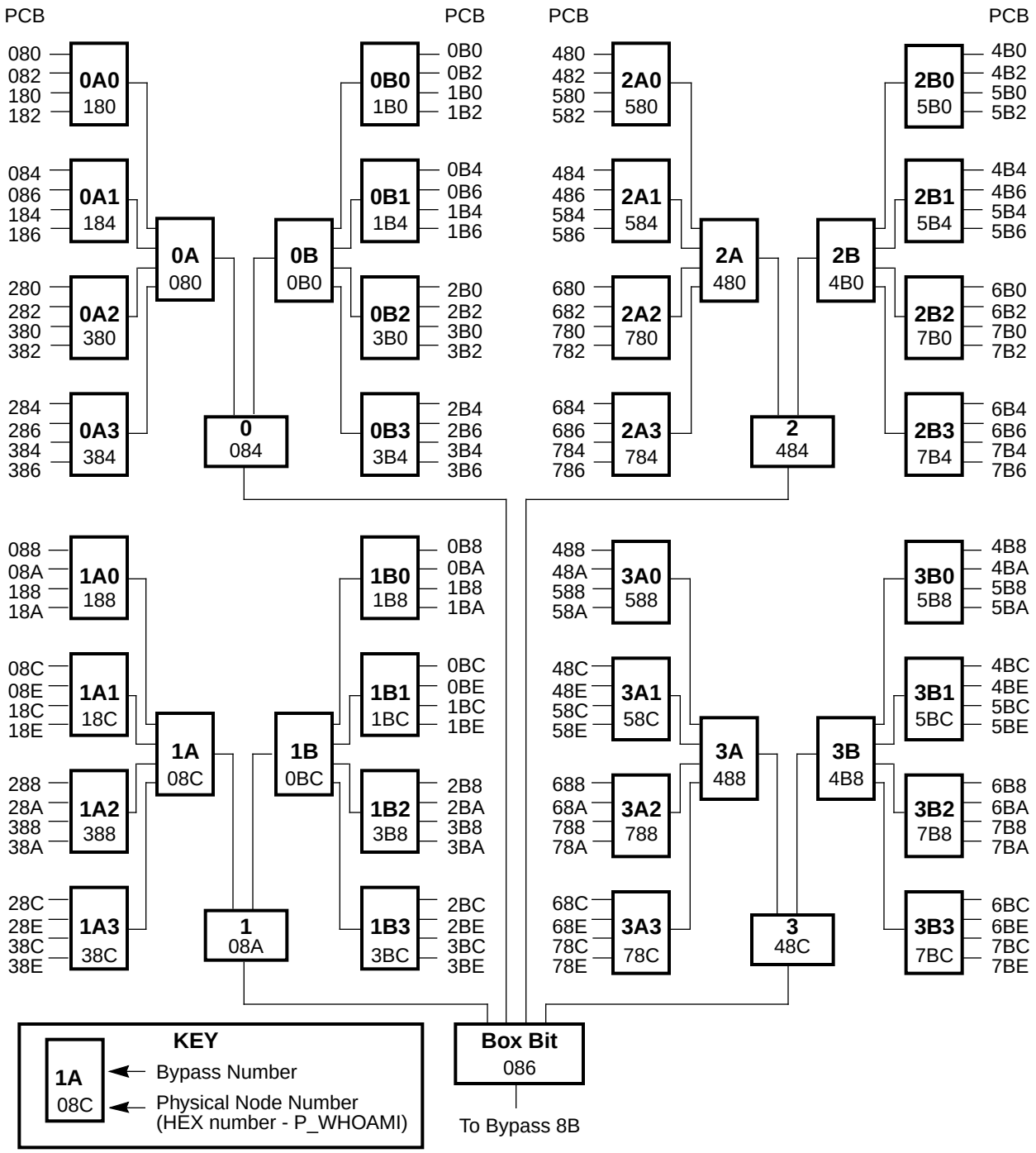
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 18. Barrier Synchronization Circuit 0 in CRAY T3D MC2048 Cabinet 0



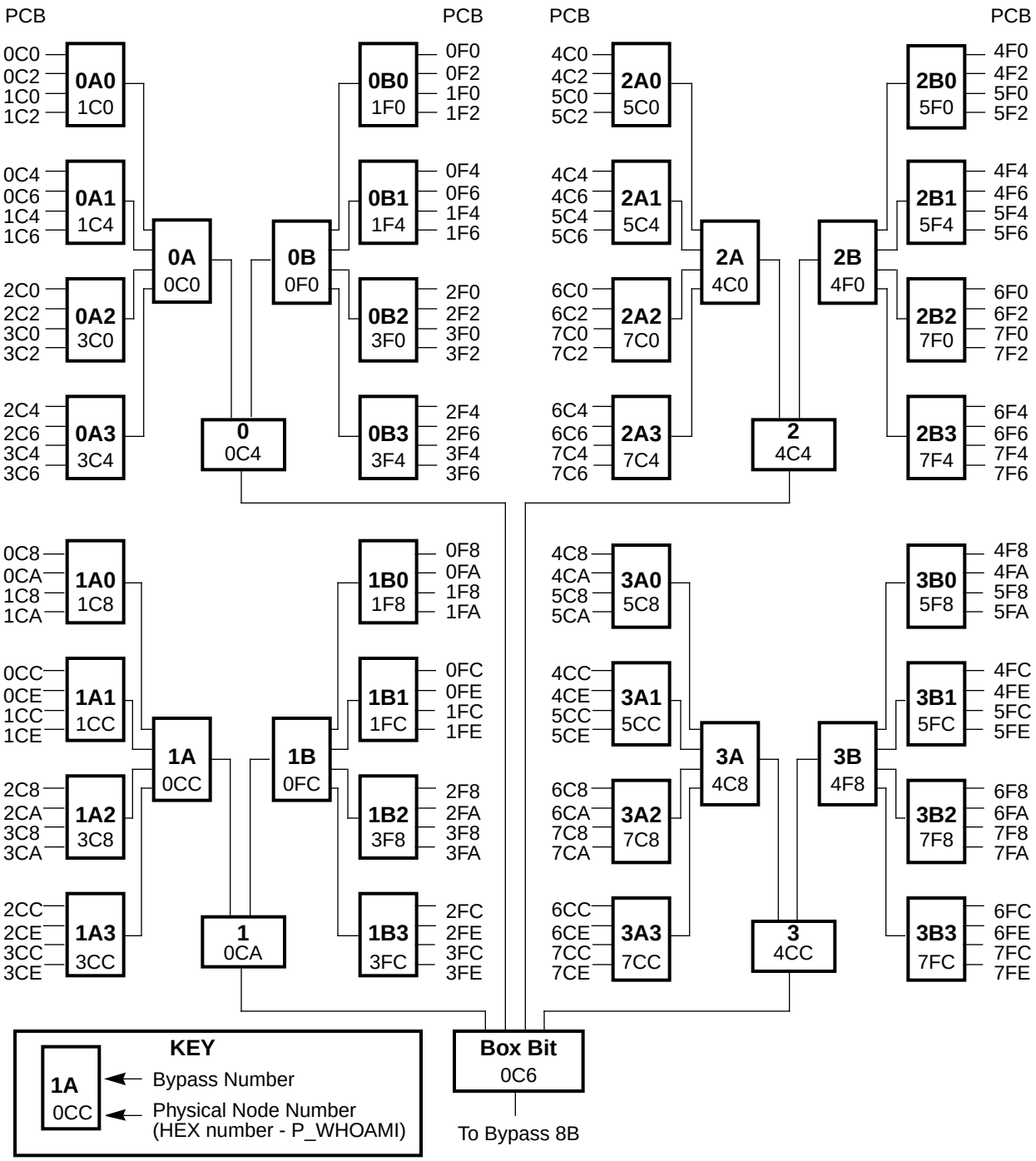
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 19. Barrier Synchronization Circuit 0 in CRAY T3D MC2048 Cabinet 1



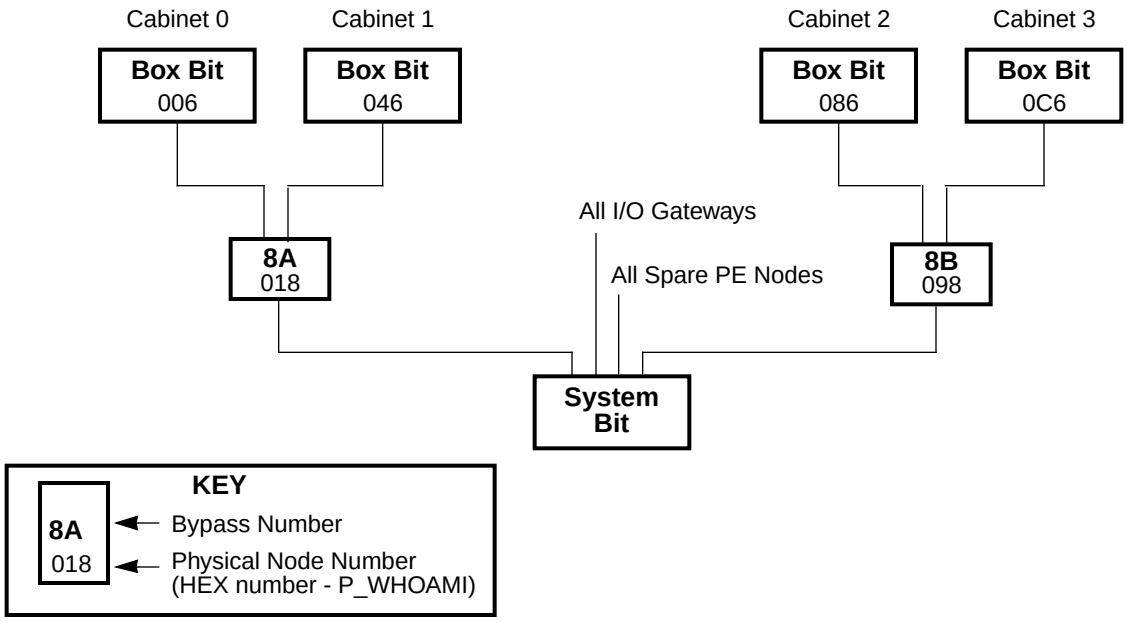
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 20. Barrier Synchronization Circuit 0 in CRAY T3D MC2048 Cabinet 2



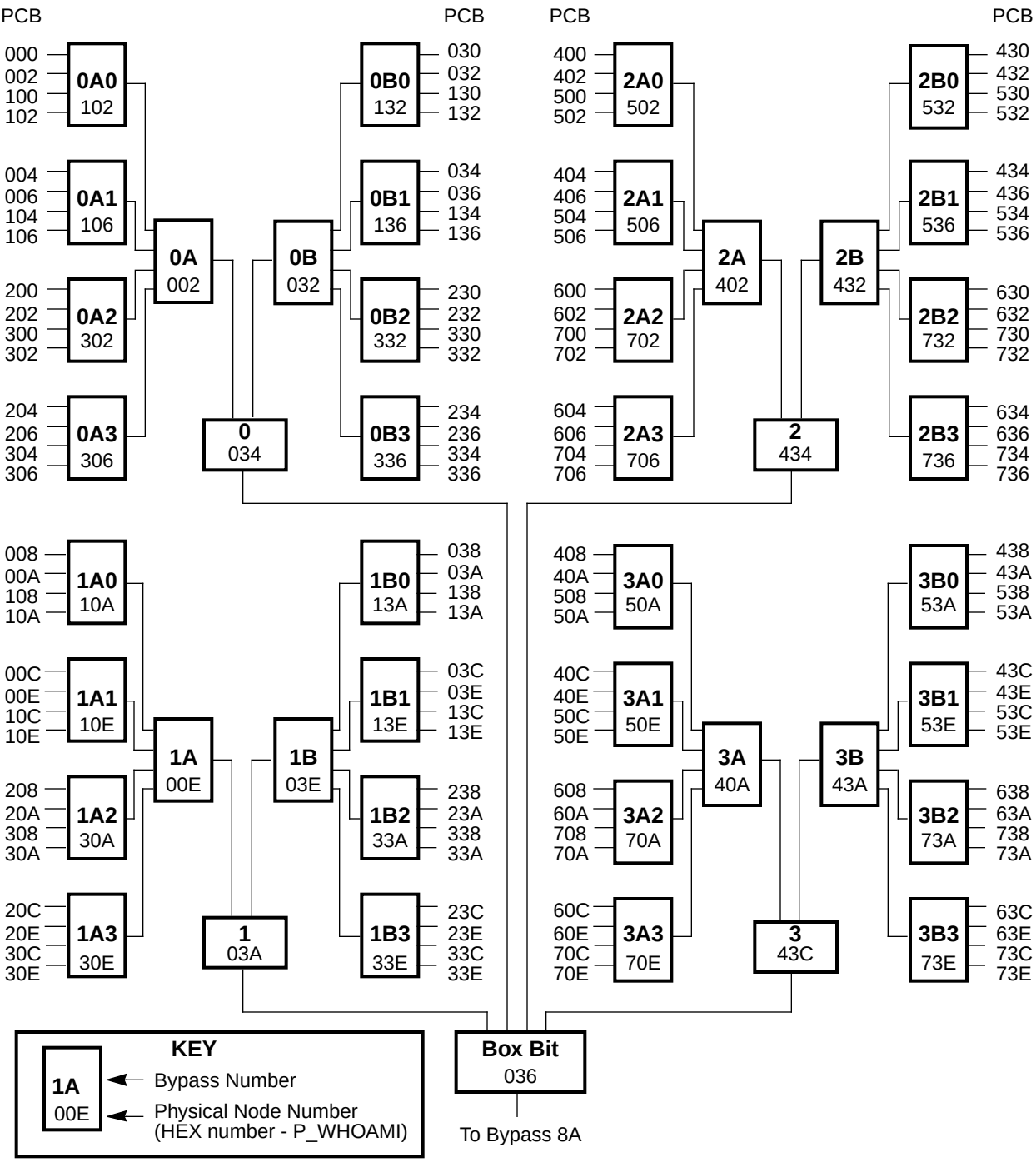
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 21. Barrier Synchronization Circuit 0 in CRAY T3D MC2048 Cabinet 3



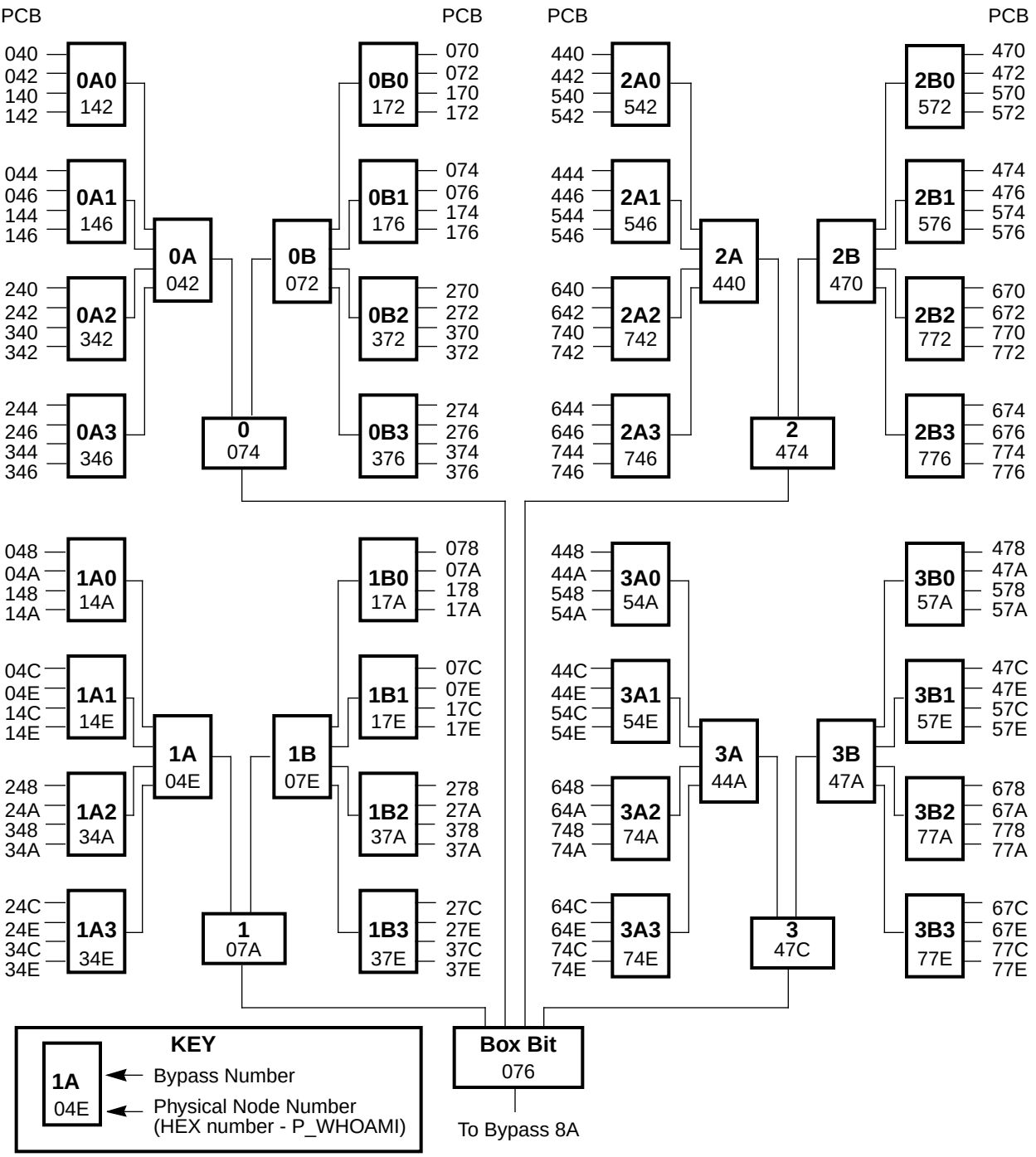
NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 22. Barrier Synchronization Circuit 0 CRAY T3D MC2048 System Bit



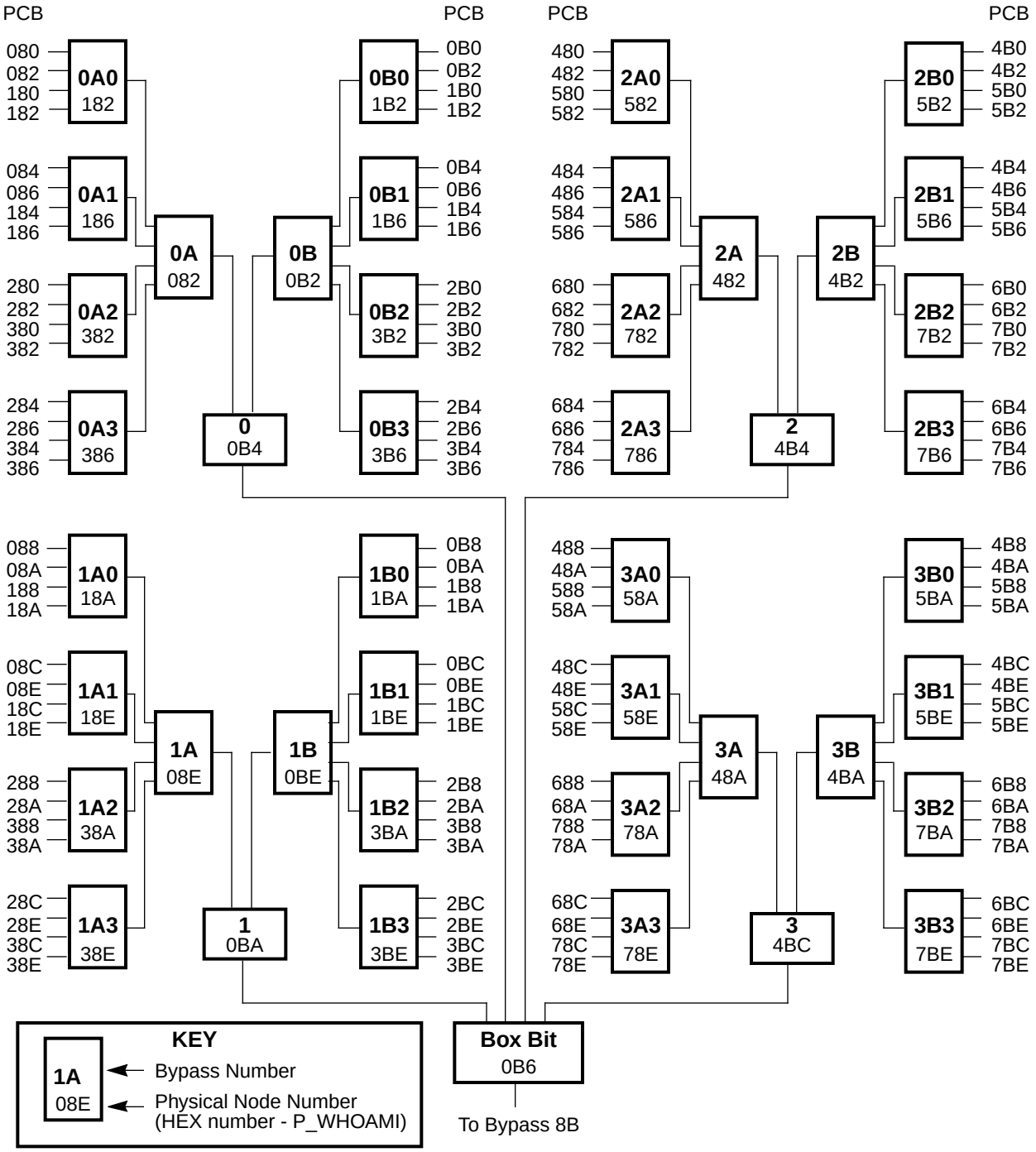
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 23. Barrier Synchronization Circuit 1 in CRAY T3D MC2048 Cabinet 0



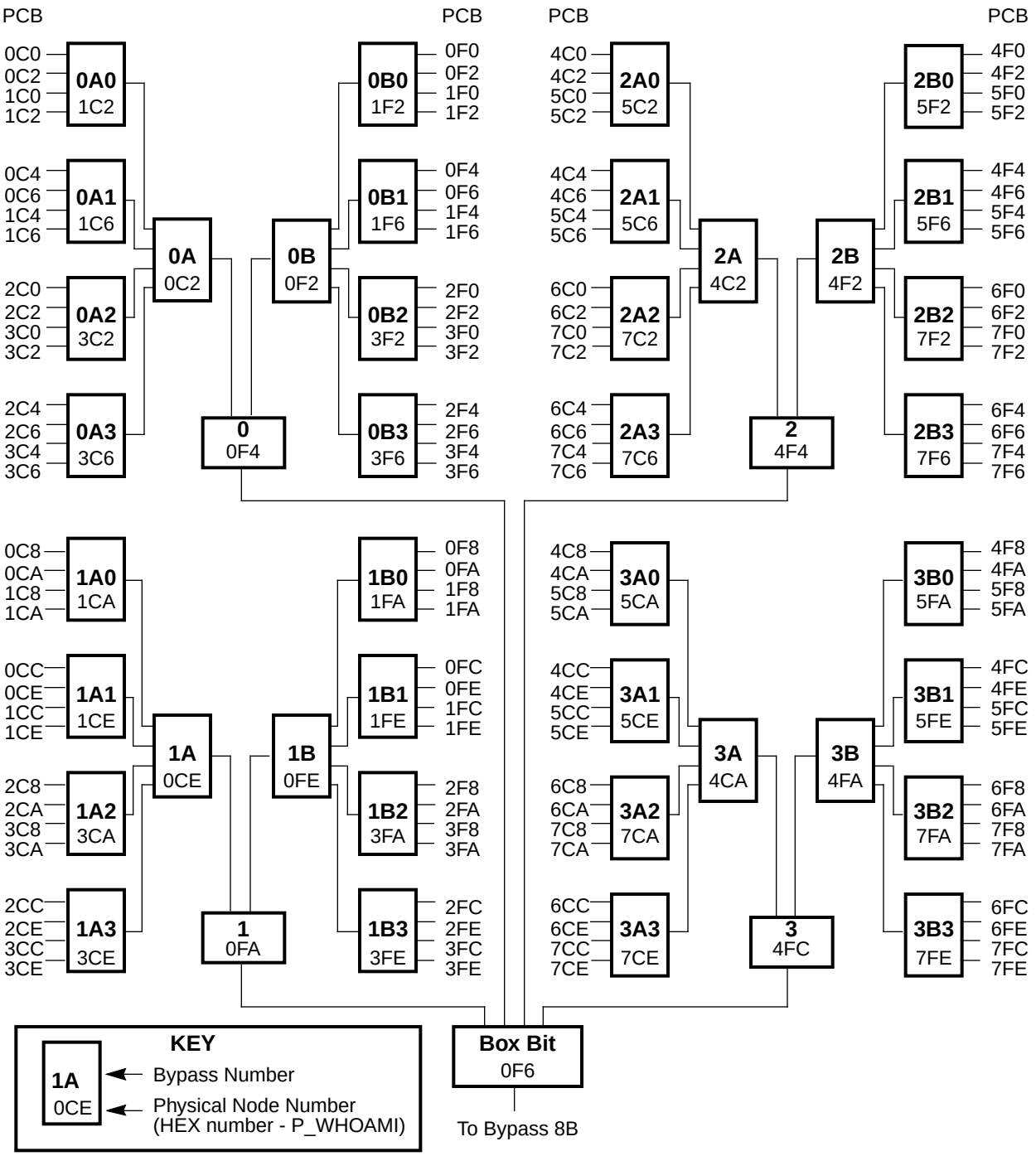
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 24. Barrier Synchronization Circuit 1 in CRAY T3D MC2048 Cabinet 1



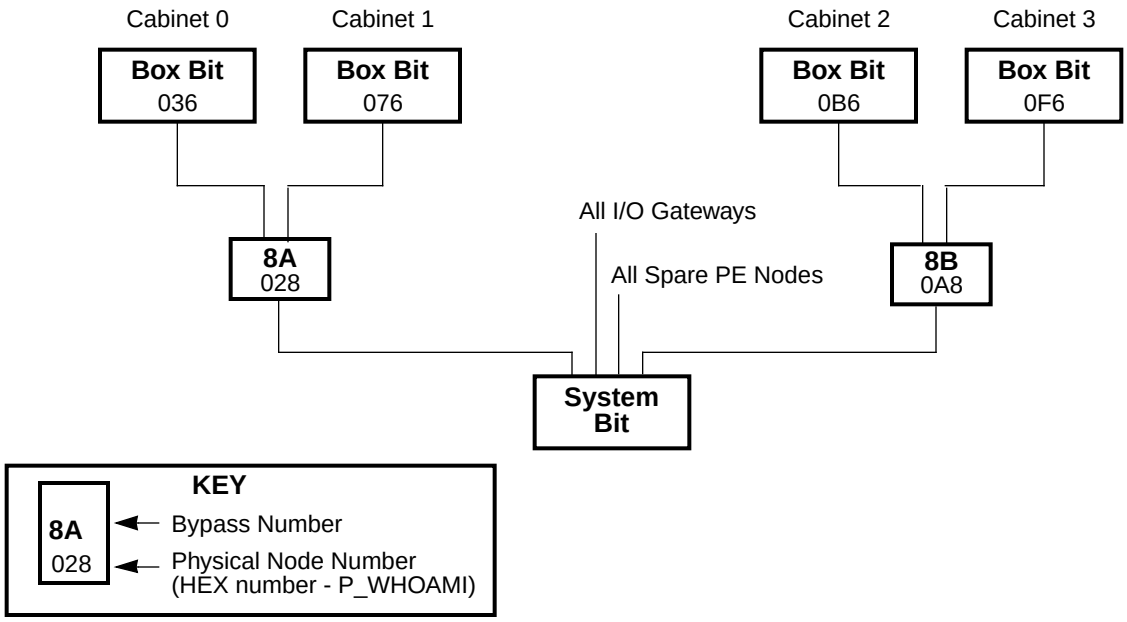
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 25. Barrier Synchronization Circuit 1 in CRAY T3D MC2048 Cabinet 2



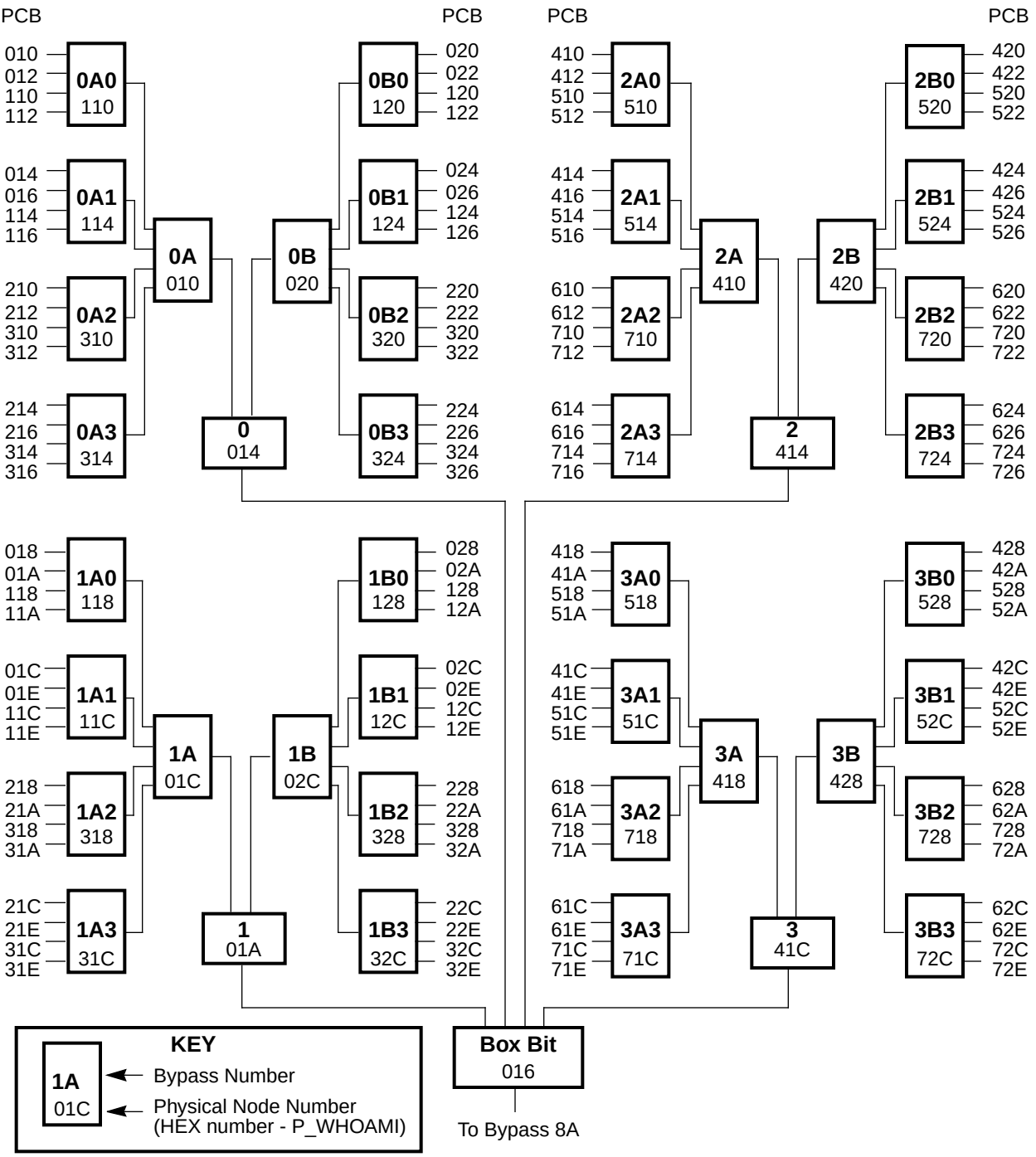
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 26. Barrier Synchronization Circuit 1 in CRAY T3D MC2048 Cabinet 3



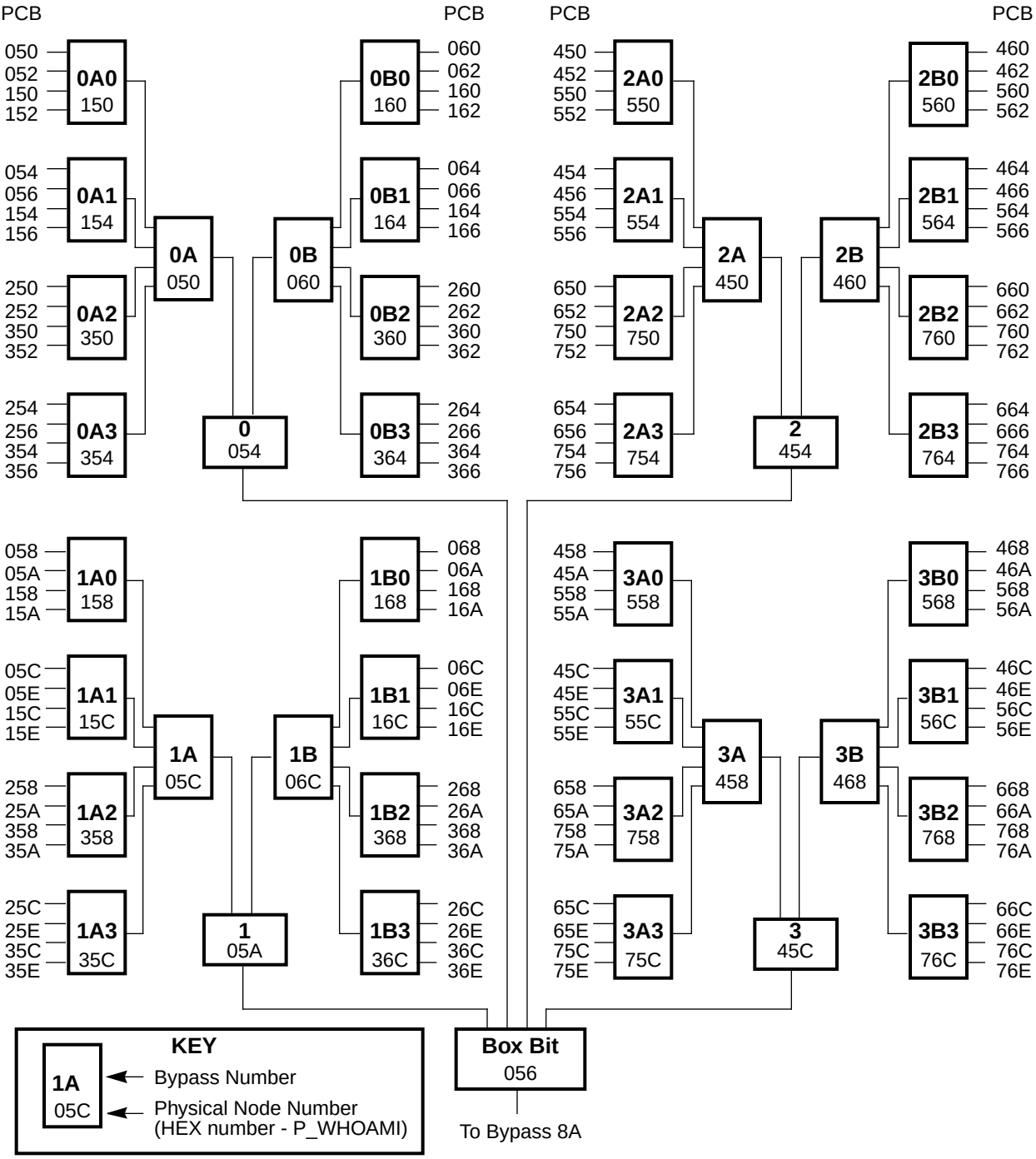
NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 27. Barrier Synchronization Circuit 1 CRAY T3D MC2048 System Bit



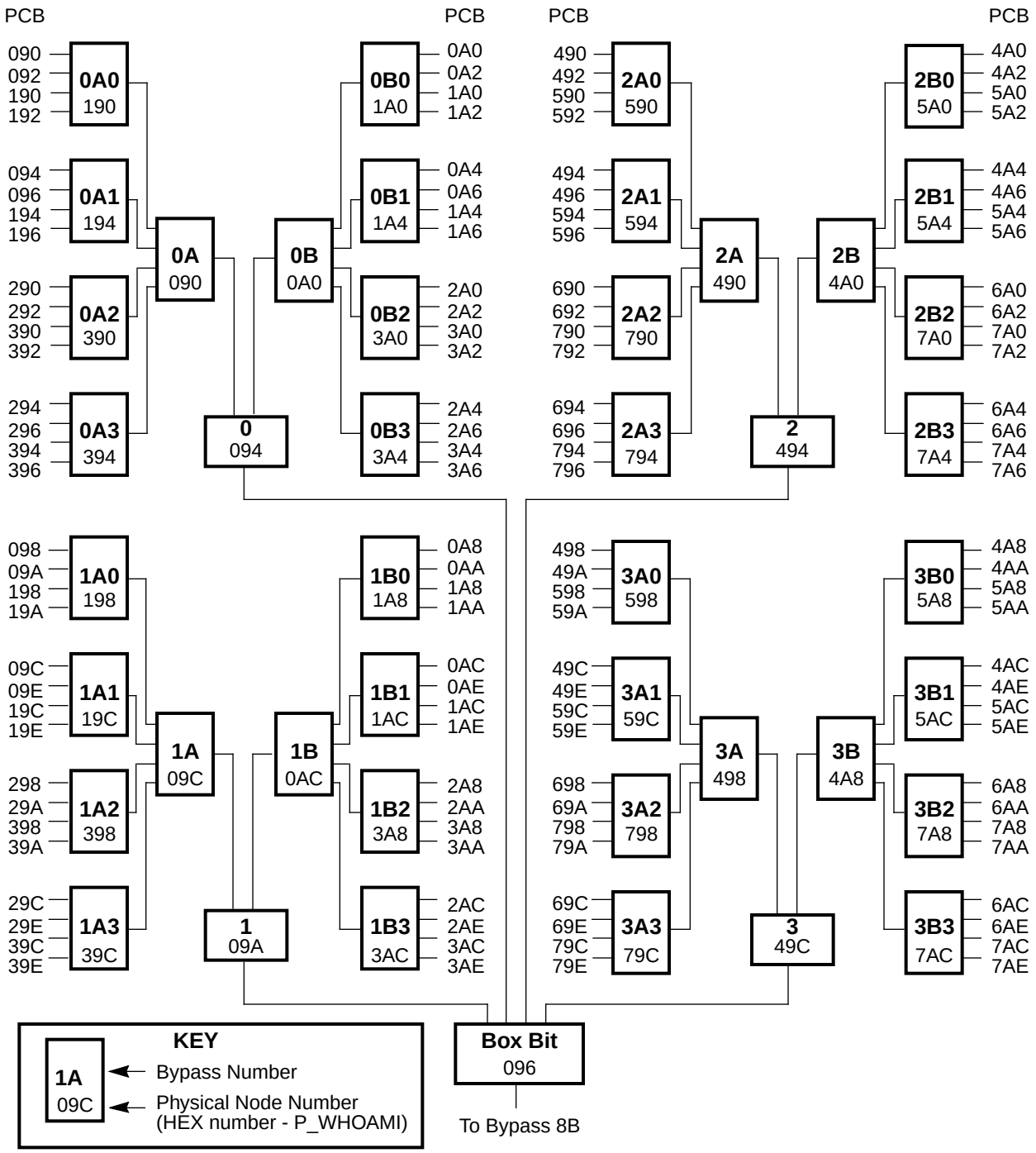
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 28. Barrier Synchronization Circuit 2 in CRAY T3D MC2048 Cabinet 0



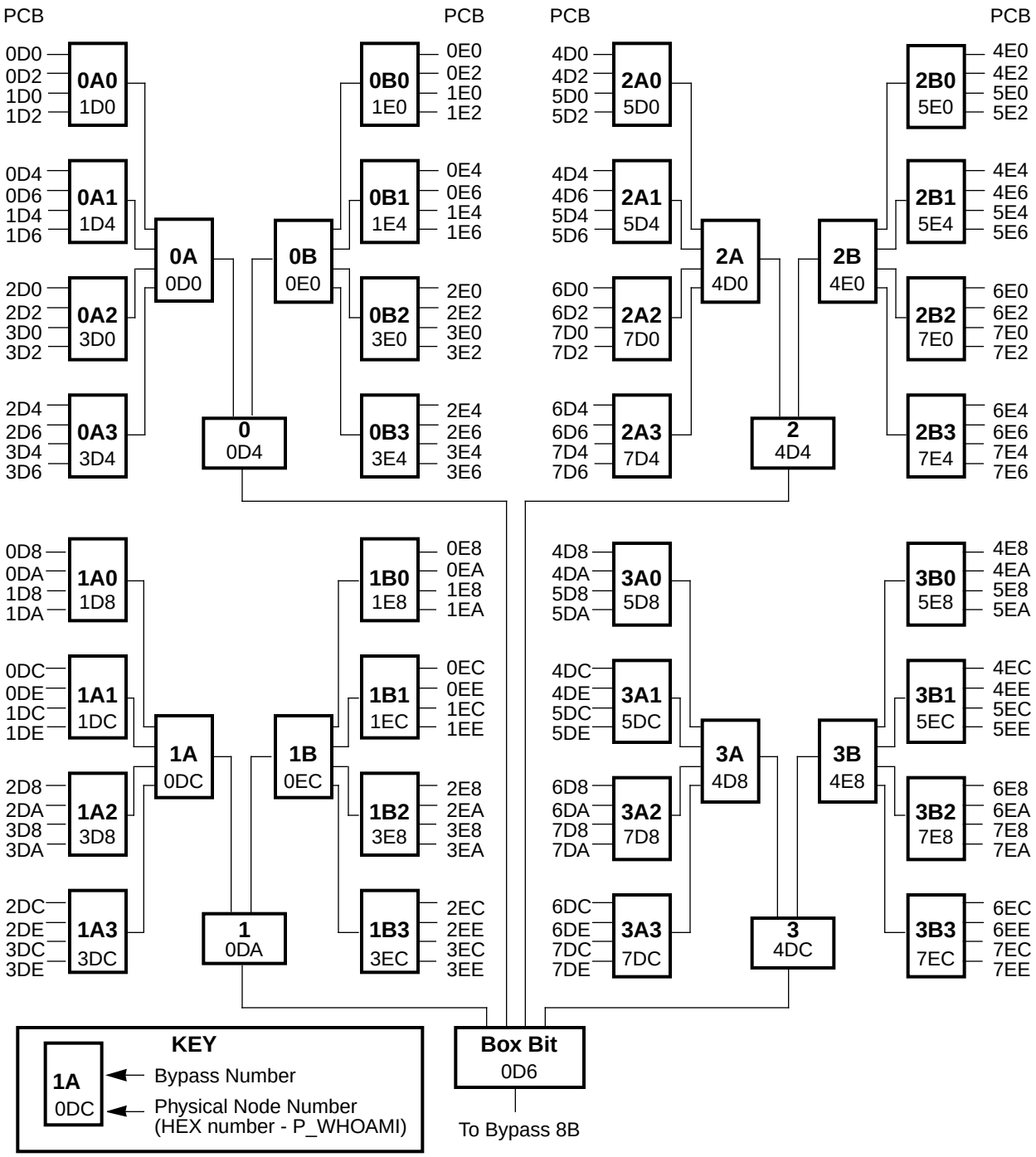
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 29. Barrier Synchronization Circuit 2 in CRAY T3D MC2048 Cabinet 1



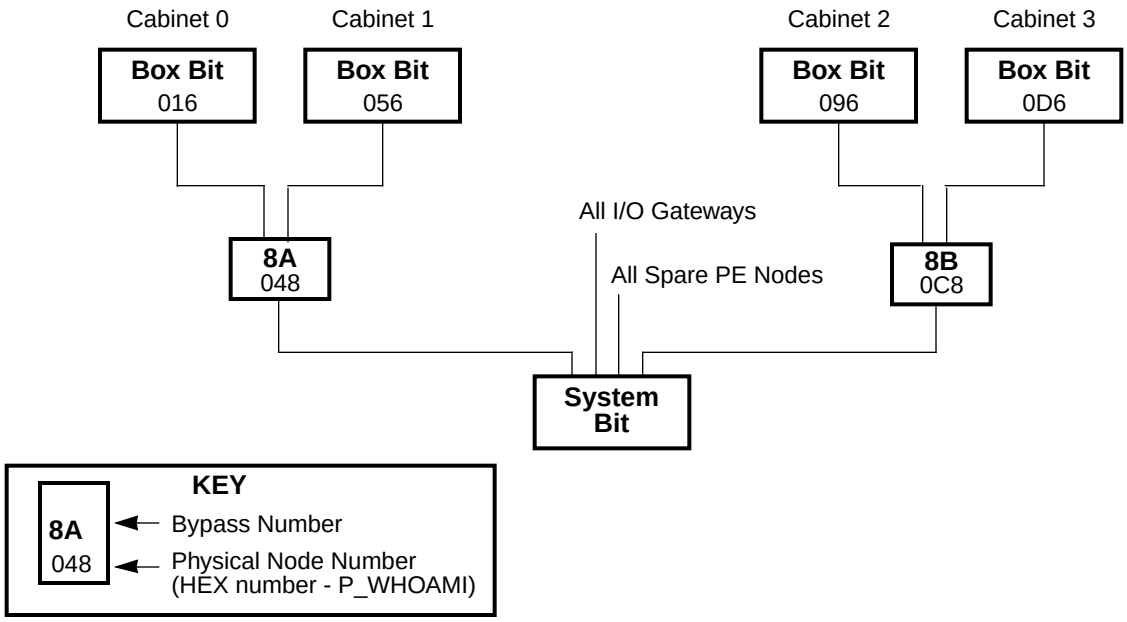
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 30. Barrier Synchronization Circuit 2 in CRAY T3D MC2048 Cabinet 2



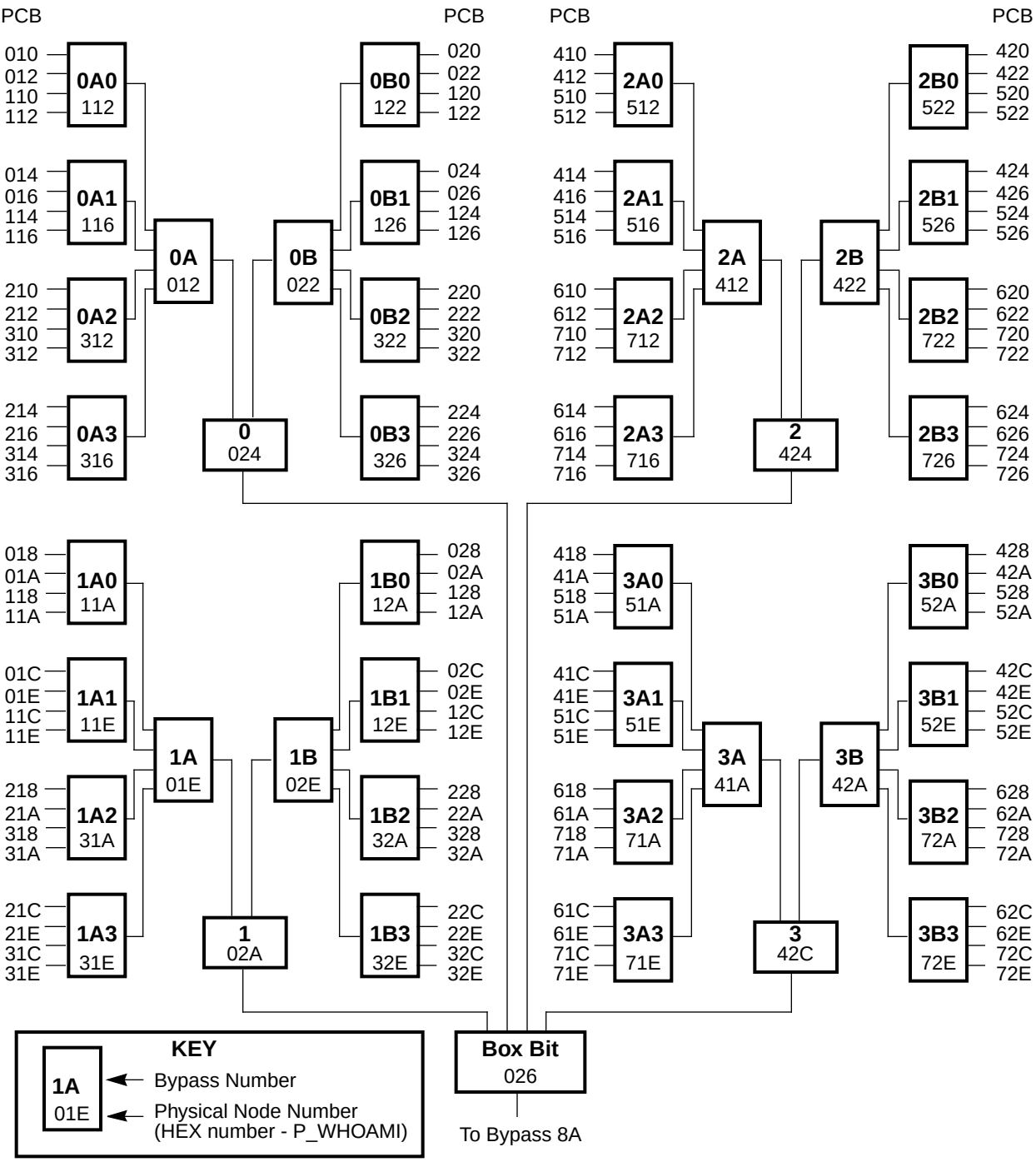
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 31. Barrier Synchronization Circuit 2 in CRAY T3D MC2048 Cabinet 3



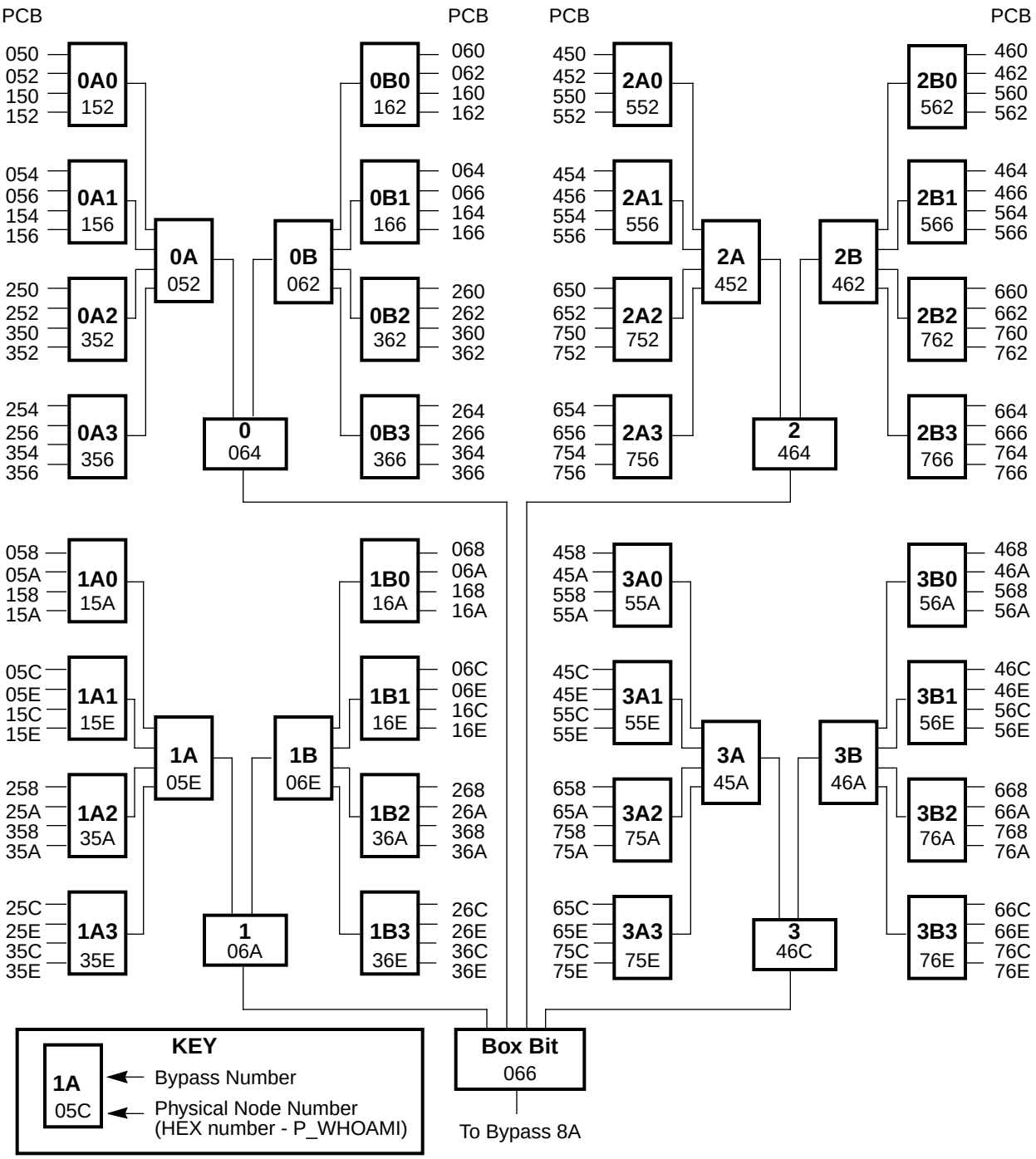
NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 32. Barrier Synchronization Circuit 2 CRAY T3D MC2048 System Bit



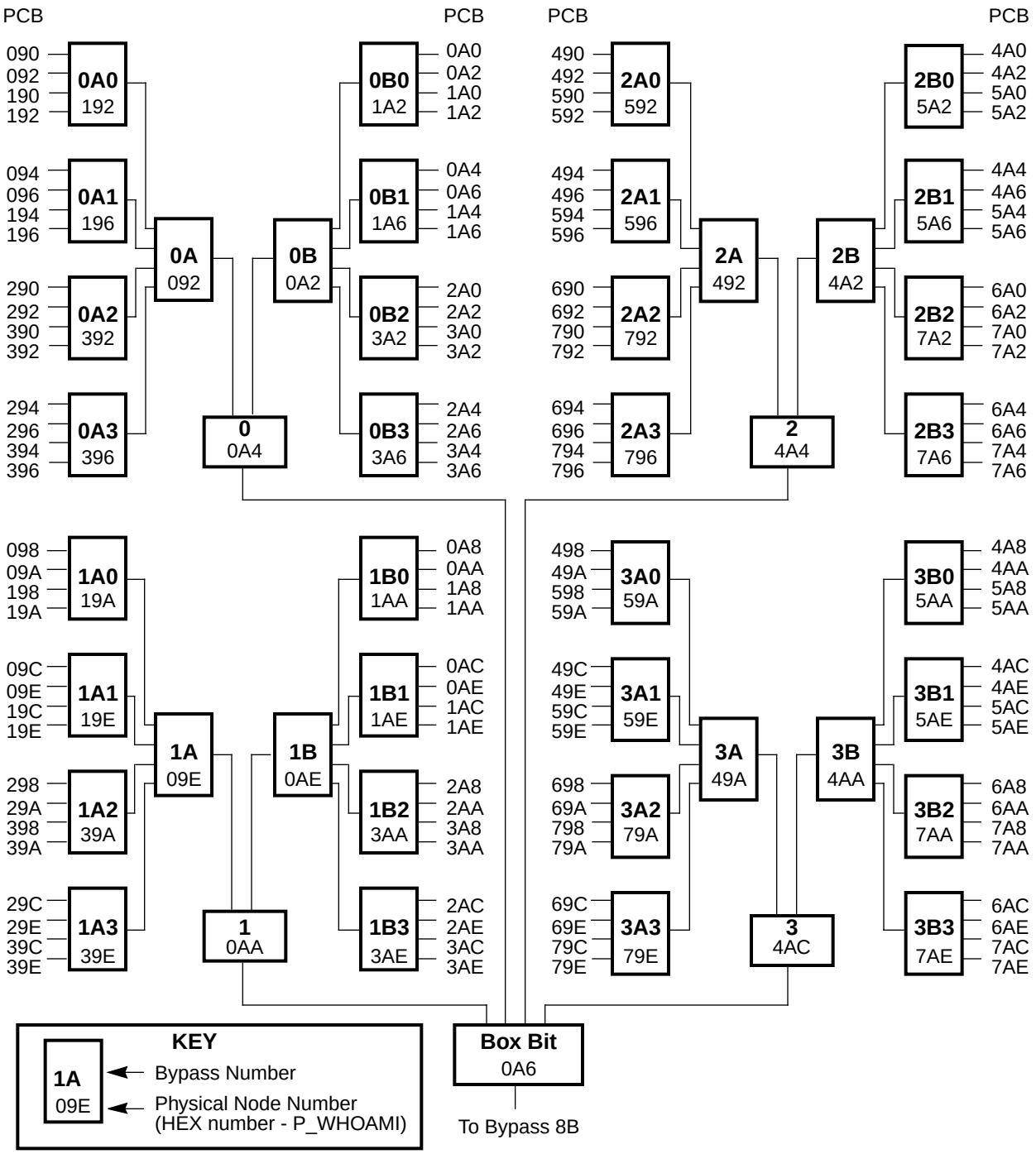
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 33. Barrier Synchronization Circuit 3 in CRAY T3D MC2048 Cabinet 0



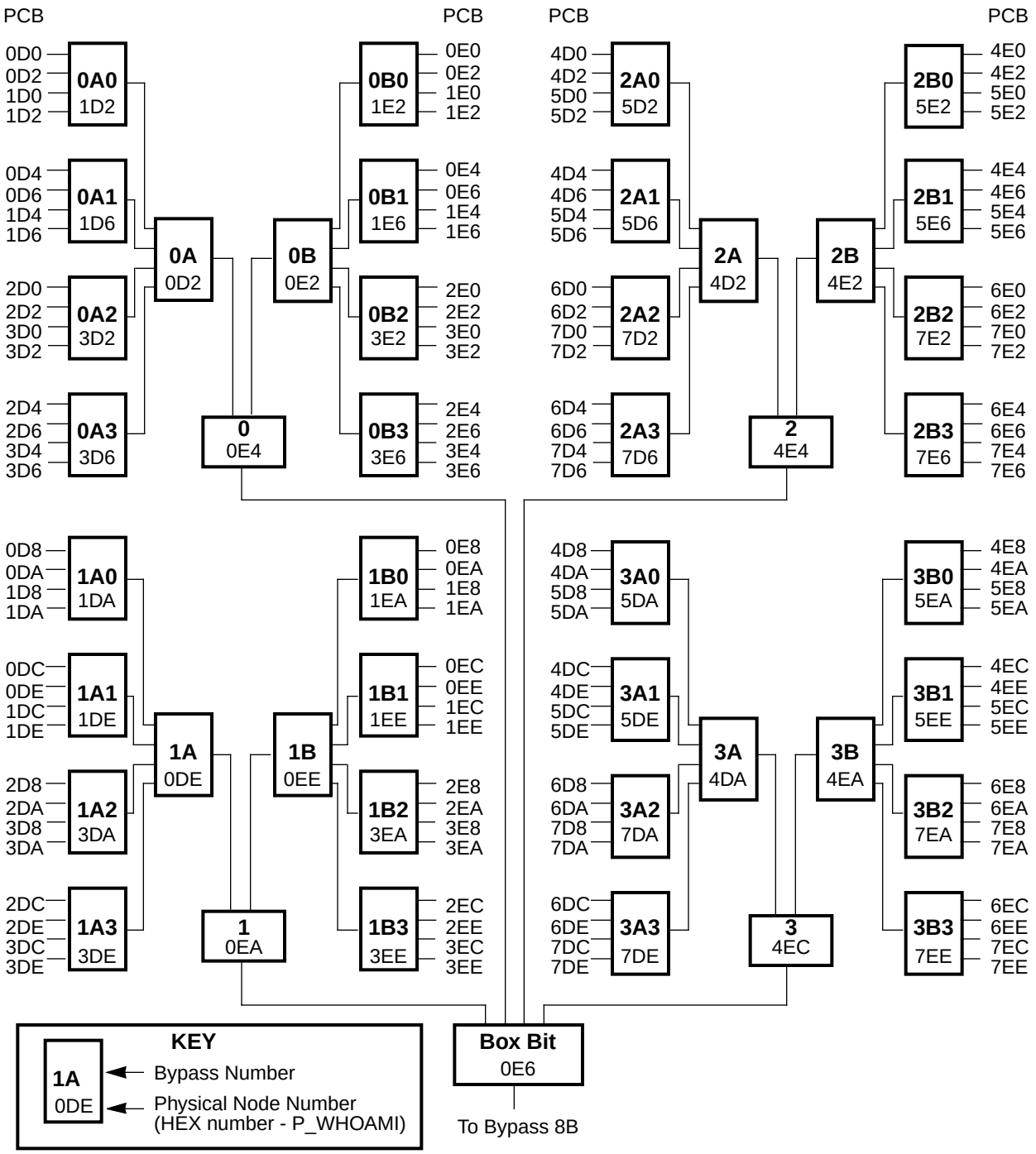
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 34. Barrier Synchronization Circuit 3 in CRAY T3D MC2048 Cabinet 1



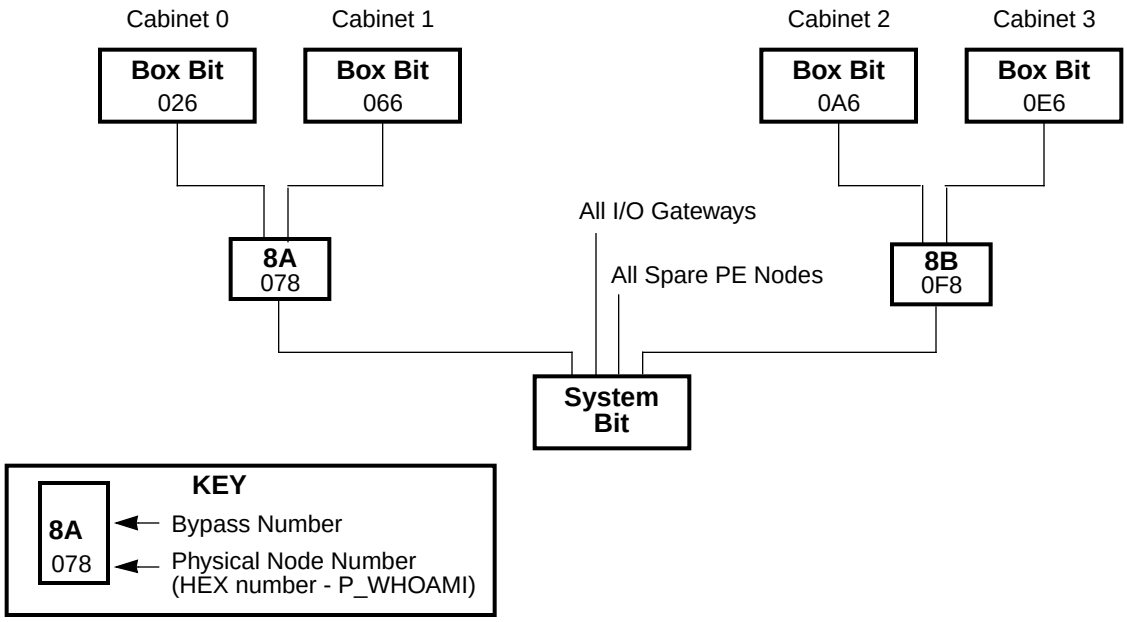
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 35. Barrier Synchronization Circuit 3 in CRAY T3D MC2048 Cabinet 2



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 36. Barrier Synchronization Circuit 3 in CRAY T3D MC2048 Cabinet 3



NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 37. Barrier Synchronization Circuit 3 CRAY T3D MC2048 System Bit

3 CRAY T3D MC1024 System

The CRAY T3D MC1024 system contains 1,024 PEs in 512 processing element nodes and is housed in two cabinets. The following subsections describe the communication links, module layout, and barrier synchronization bypass points for the CRAY T3D MC1024 system.

NOTE: Throughout this document, physical PE numbers are represented as three-digit hexadecimal numbers that correspond to the physical PE numbers in the P_WHOAMI registers. For example, a PE may have a physical PE number of $10B_{16}$.

NOTE: Throughout this document, physical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $10A_{16}$ contains the physical PEs $10A_{16}$ and $10B_{16}$.

NOTE: Throughout this document, logical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a L_WHOAMI register with bit 2^0 set to 0. For example, logical node $10A_{16}$ contains the logical PEs $10A_{16}$ and $10B_{16}$.

3.1 CRAY T3D MC1024 Communication Links

Figure 38 shows the physical communication links between nodes in the Y dimension. Note that the nodes are not connected in sequential order of physical node number.

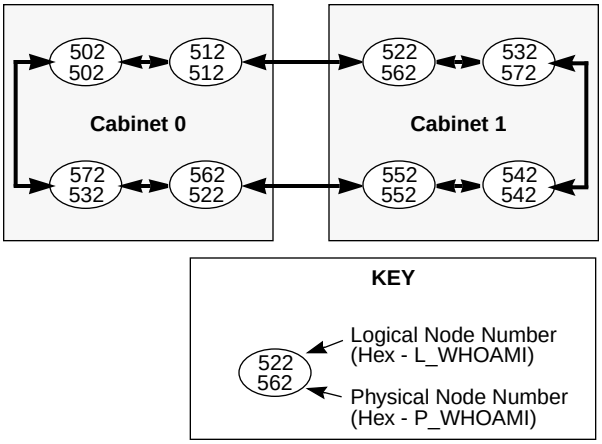


Figure 38. CRAY T3D MC1024 Y-dimension Communication Links

Figure 39 shows the physical communication links between spare nodes in the Y dimension.

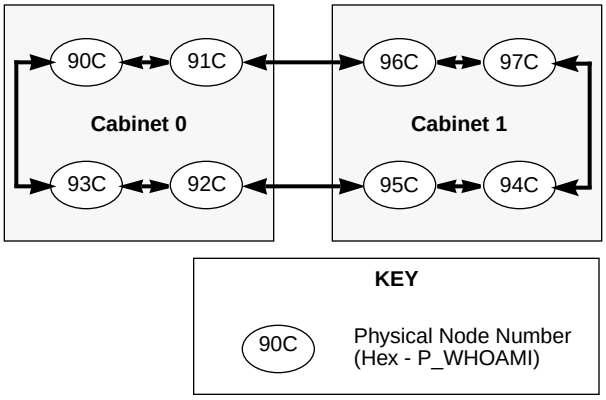


Figure 39. CRAY T3D MC1024 Spare Node Y-dimension Communication Links

Figure 40 and Figure 41 show the physical communication links between the nodes in the X and Z dimensions. For clarity, the figures do not show the communication links that complete the torus in the X and Z dimensions.

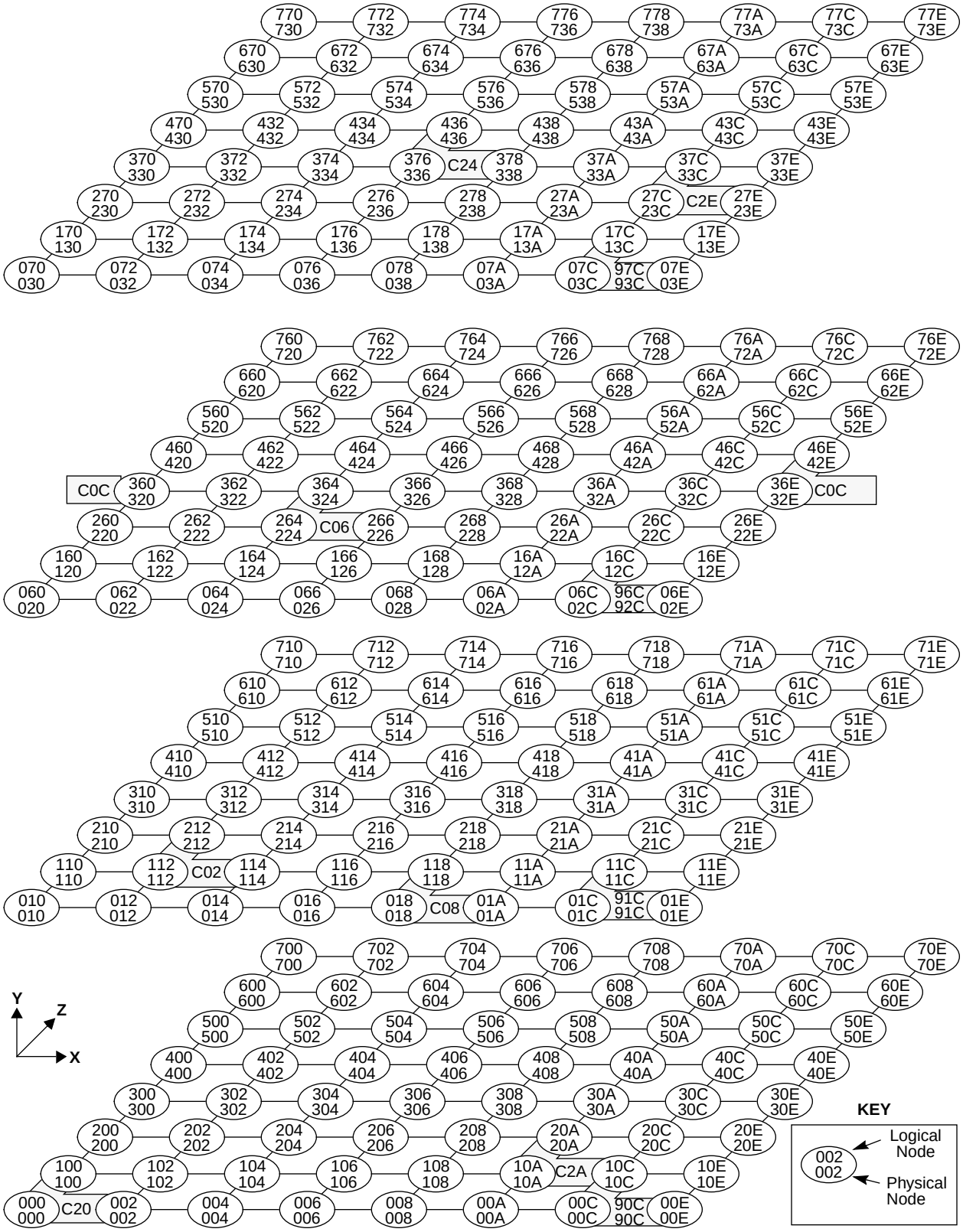


Figure 40. CRAY T3D MC1024 Cabinet 0 X- and Z-dimension Communication Links

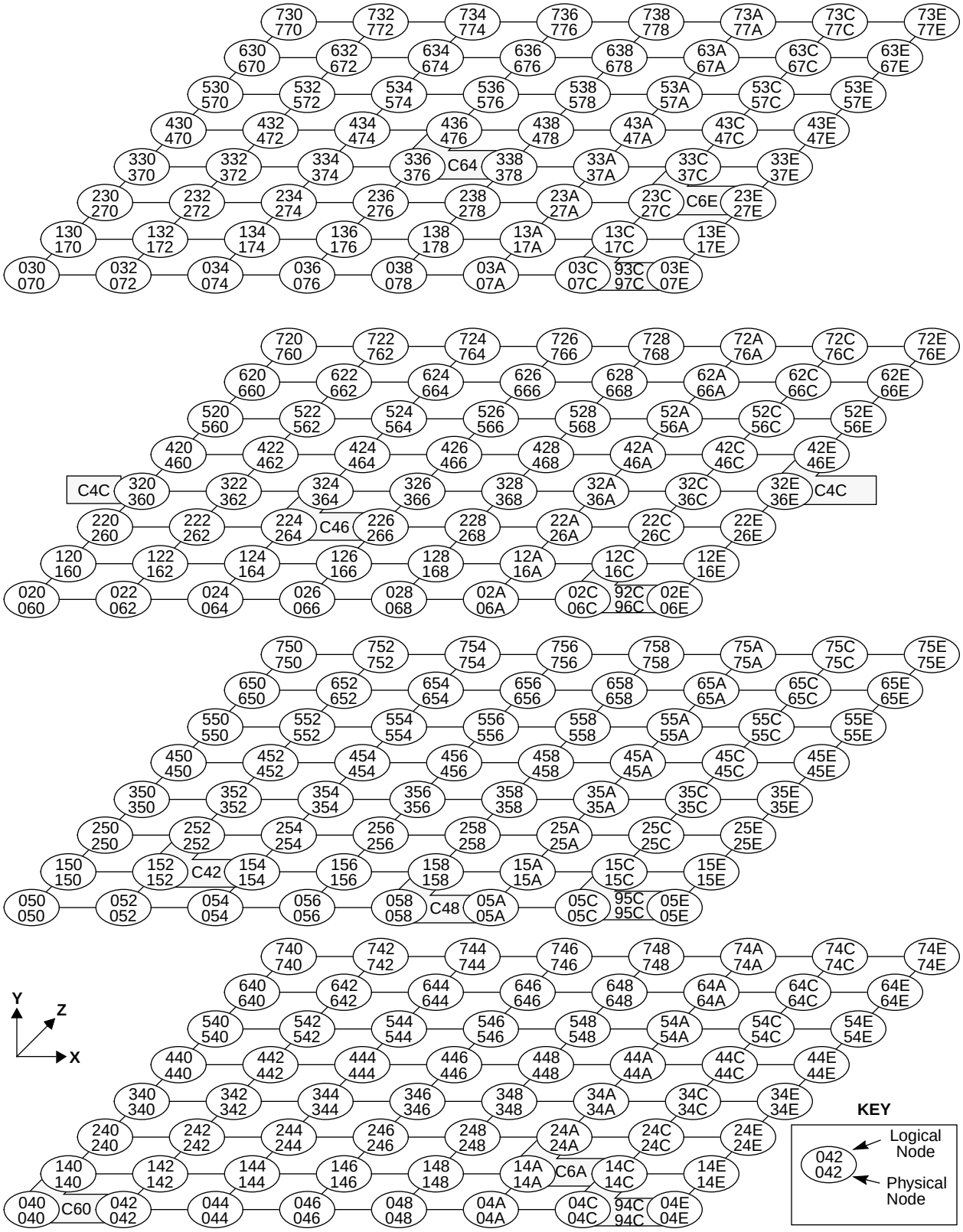


Figure 41. CRAY T3D MC1024 Cabinet 1 X- and Z-dimension Communication Links

3.2 CRAY T3D MC1024 Module Layout

Figure 42 and Figure 43 show the module layout and physical node locations in each of the two CRAY T3D MC1024 system cabinets. Each figure represents the physical node number as a three-digit hexadecimal number that is equivalent to the number read from the P_WHOAMI register with bit 2^0 set to 0. For example, physical node 002_{16} contains the physical PEs 002_{16} and 003_{16}.

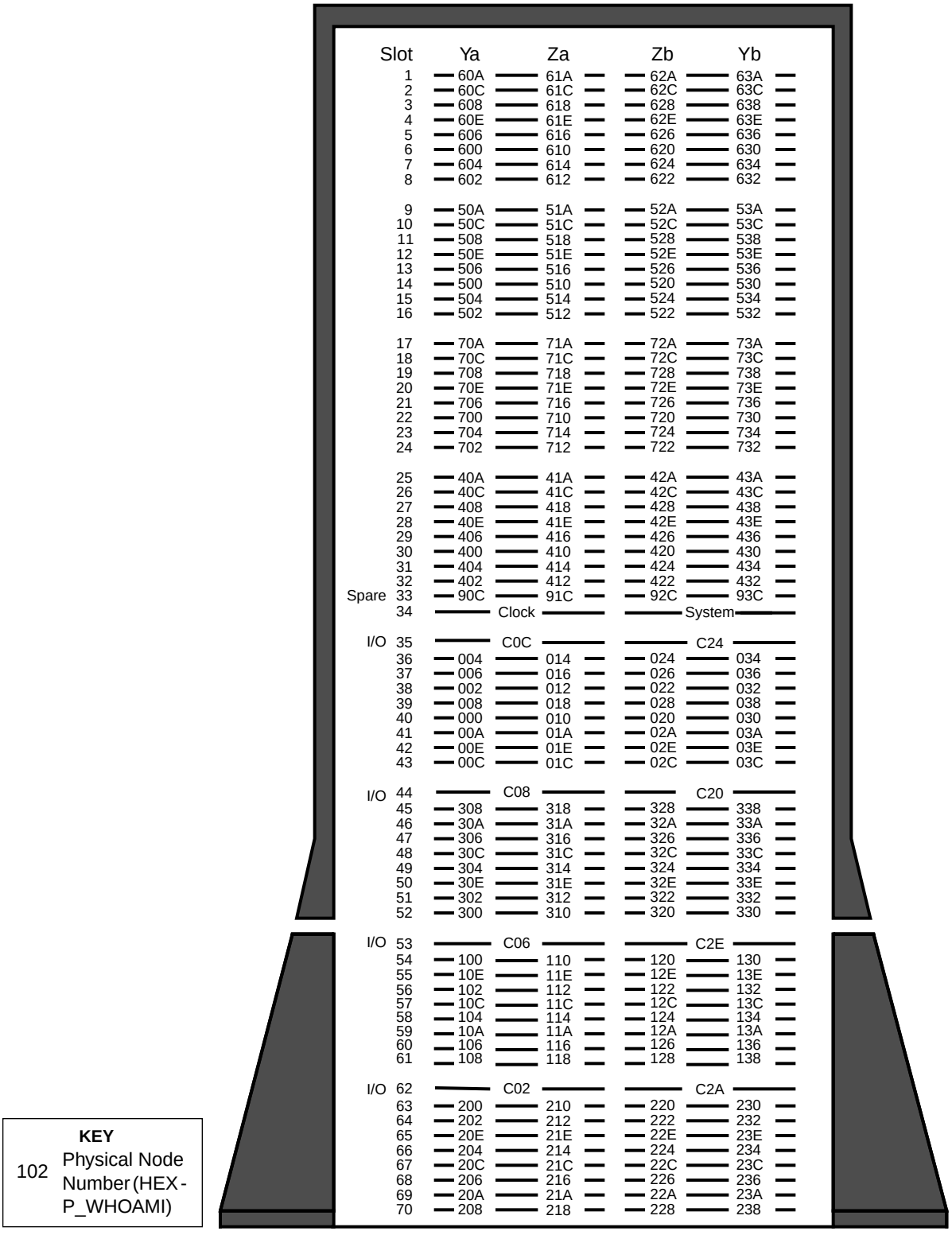


Figure 42. CRAY T3D MC1024 Cabinet 0 Module Layout

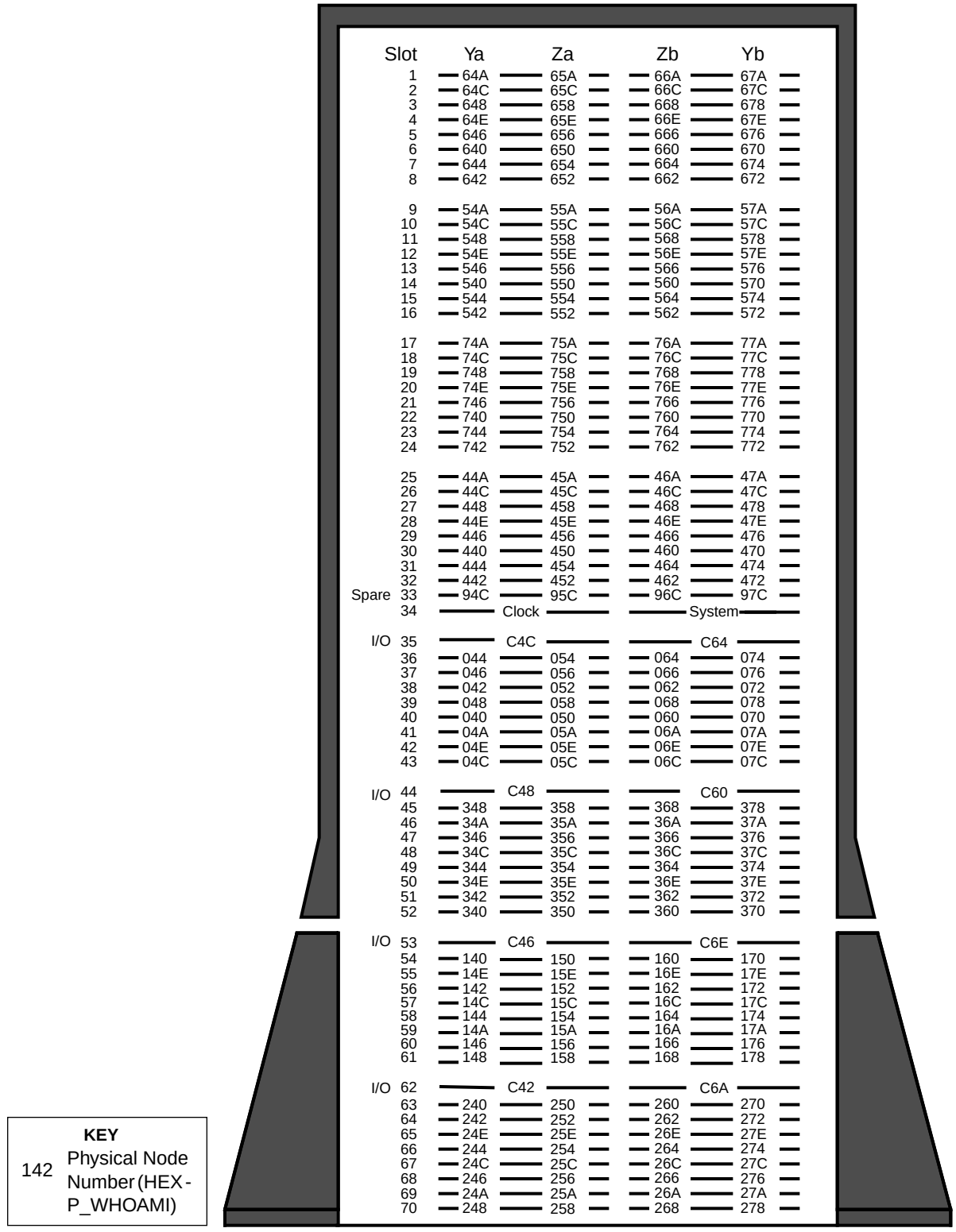


Figure 43. CRAY T3D MC1024 Cabinet 1 Module Layout

3.3 CRAY T3D MC1024 Barrier Synchronization Circuits

Figure 44 through Figure 55 show the barrier synchronization bypass points for all four physical barrier synchronization circuits in each of the two CRAY T3D MC1024 system cabinets. In these figures, the printed circuit board (PCB) bypass points and all other bypass points are shown.

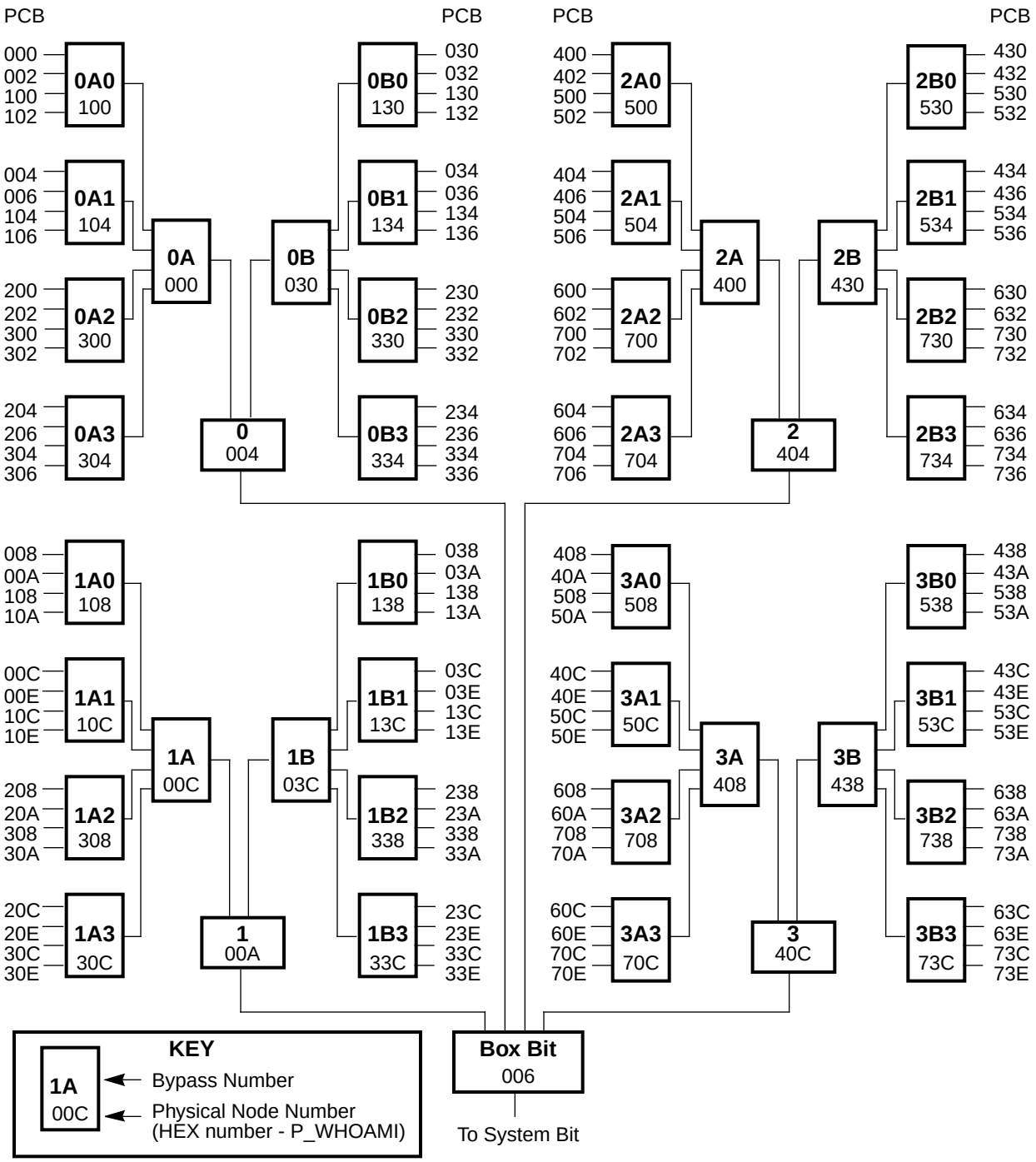
The PCB bypass points are controlled by bit 2^{11} or bit 2^{12} of the network mode register (NODE_CSR). Every processing element node PCB contains four PCB bypass points (one for each physical barrier synchronization circuit).

Each PCB bypass point is given a name that corresponds to the physical node that controls the bypass point. For example, the PCB bypass point 402 in barrier synchronization circuit 0 is located on the PCB that contains physical PEs 402_{16}, 403_{16}, 412_{16}, and 413_{16}. This bypass is controlled by setting bit 2^{11} of the NODE_CSR in physical node 402 (which contains physical PEs 402_{16} and 403_{16}) to the appropriate value.

When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 0, the output of the AND gate in a PCB bypass point is redirected to the fanout block in the bypass point. When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 1, the output of the AND gate in a PCB bypass point is directed to a second-level bypass point.

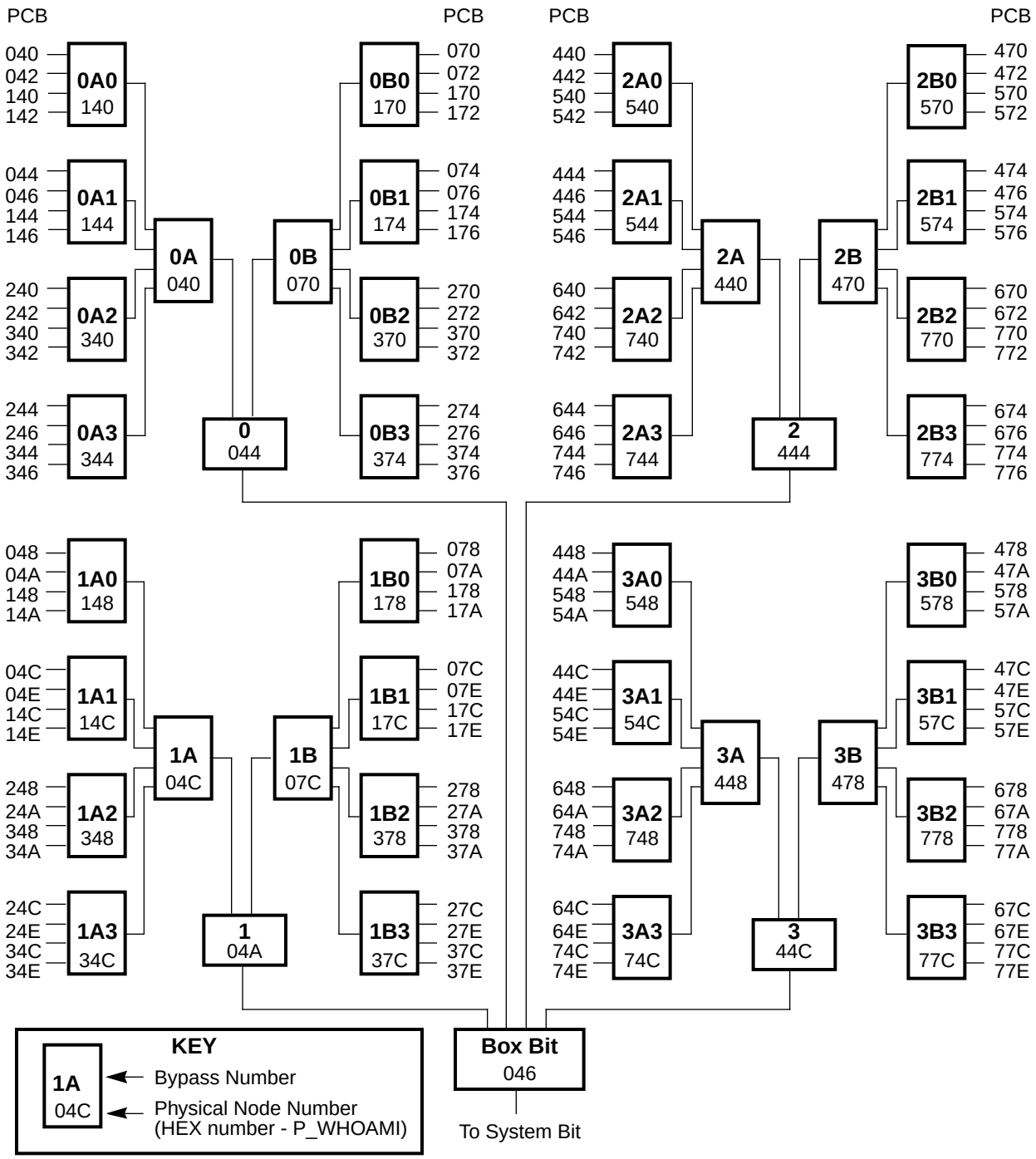
The other bypass points shown in the following figures are controlled by bit 2^{13} of the NODE_CSR. For example, bypass point 0A in barrier synchronization circuit 0 of cabinet 0 is controlled by setting bit 2^{13} of the NODE_CSR in physical node 000_{16} (which contains physical PEs 000_{16} and 001_{16}) to the appropriate value.

When bit 2^{13} of the NODE_CSR is set to 0, the output of the AND gate in the bypass point is redirected to the fanout block in the bypass point. When bit 2^{13} of the NODE_CSR is set to 1, the output of the AND gate in the bypass point is directed to the next-level bypass point.



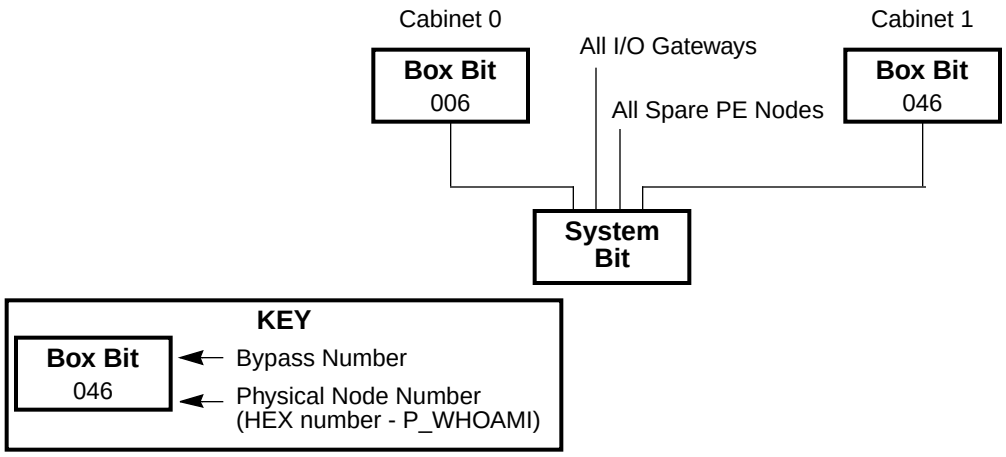
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 44. Barrier Synchronization Circuit 0 in CRAY T3D MC1024 Cabinet 0



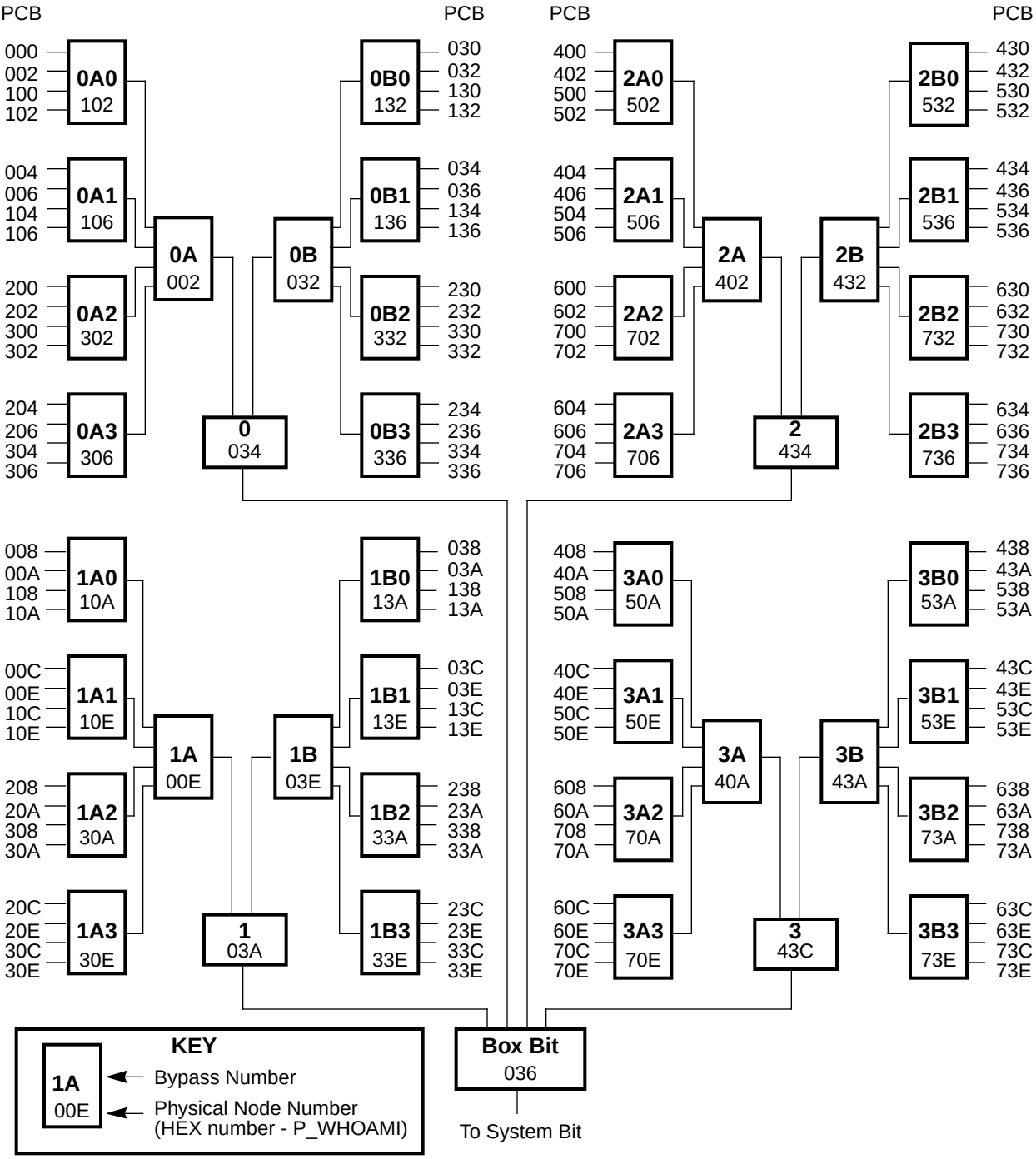
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 45. Barrier Synchronization Circuit 0 in CRAY T3D MC1024 Cabinet 1



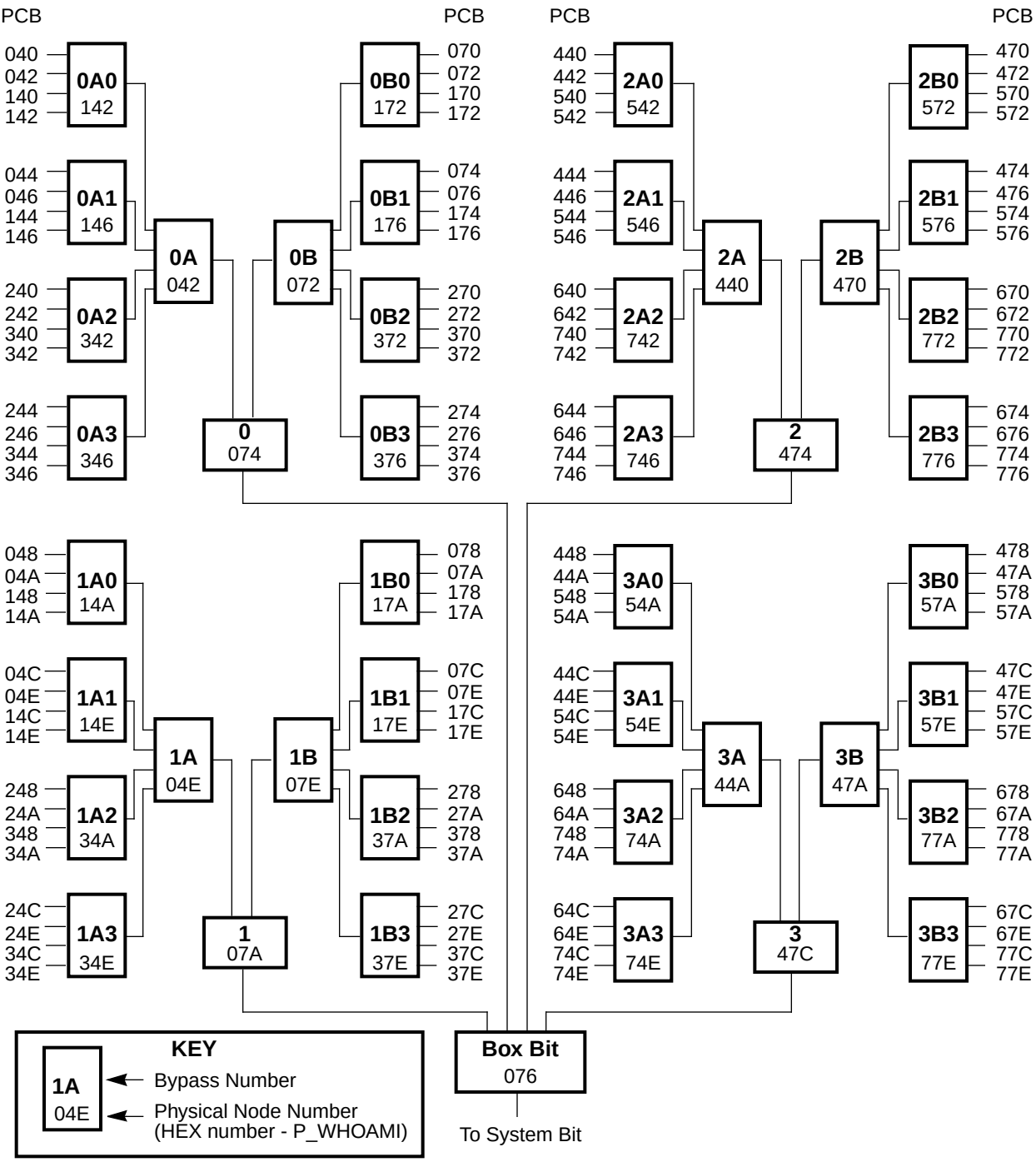
NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 46. Barrier Synchronization Circuit 0 CRAY T3D MC1024 System Bit



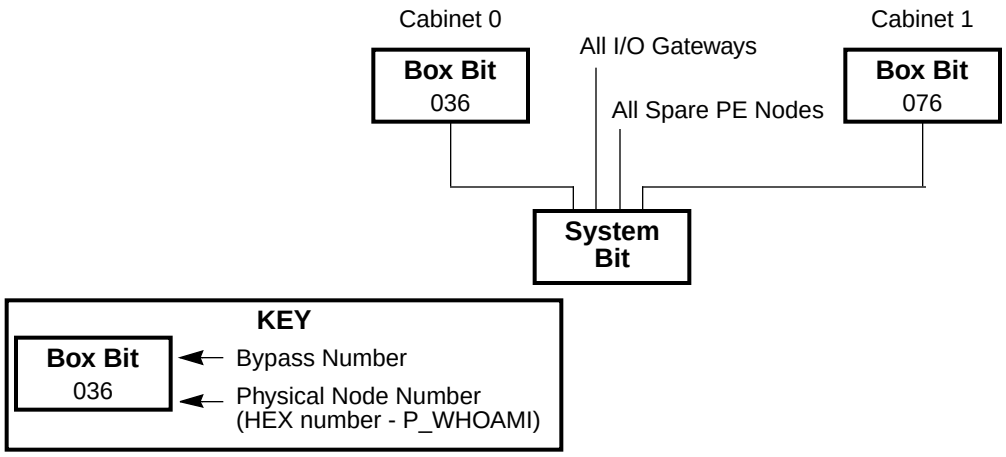
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 47. Barrier Synchronization Circuit 1 in CRAY T3D MC1024 Cabinet 0



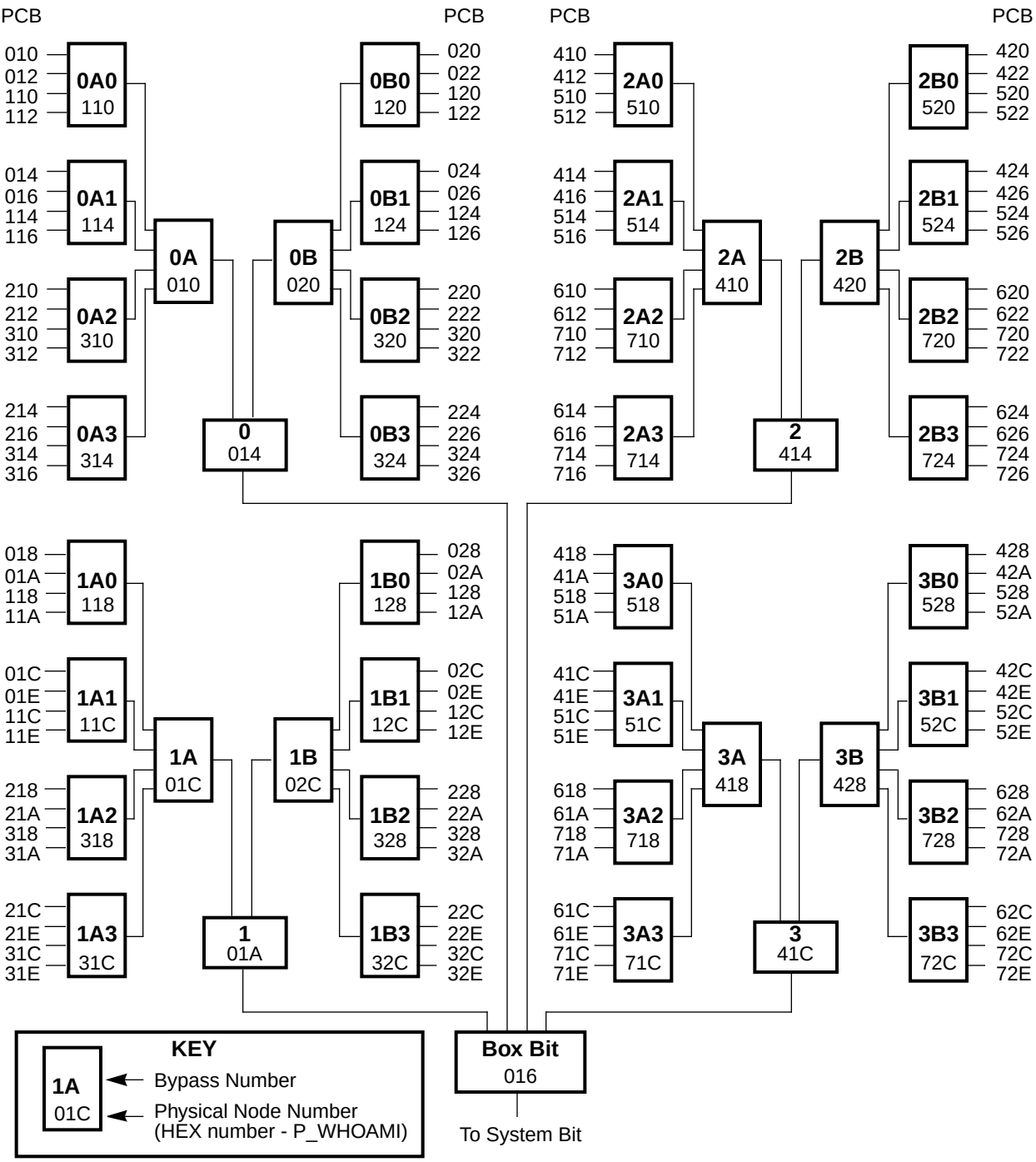
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 48. Barrier Synchronization Circuit 1 in CRAY T3D MC1024 Cabinet 1



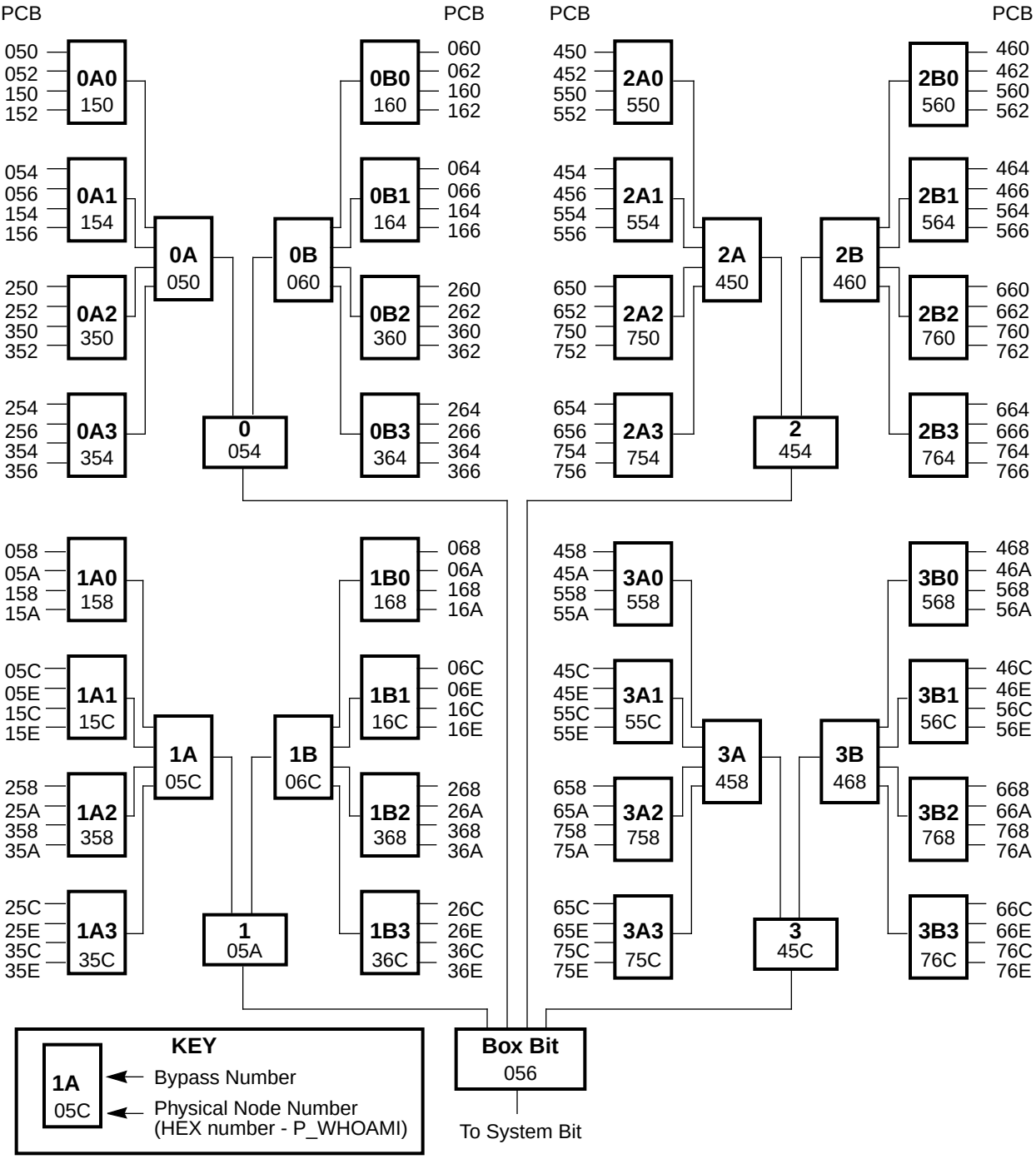
NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 49. Barrier Synchronization Circuit 1 CRAY T3D MC1024 System Bit



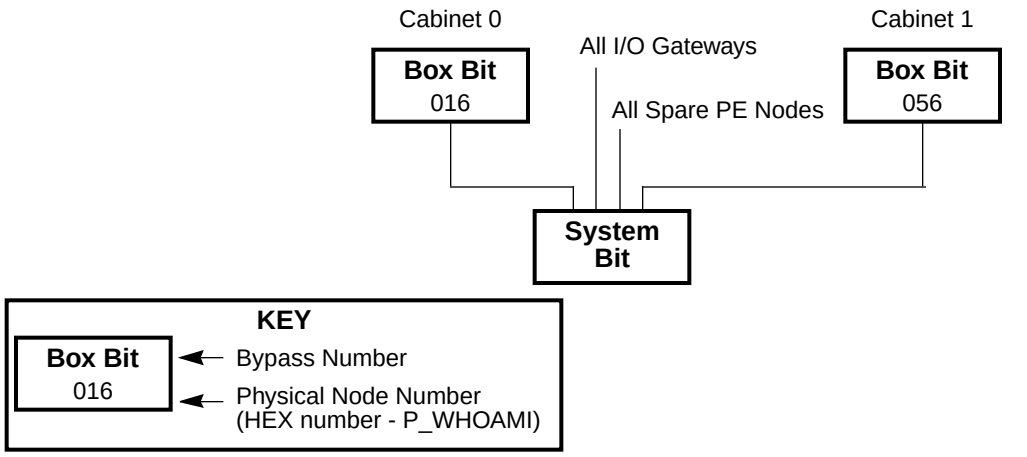
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 50. Barrier Synchronization Circuit 2 in CRAY T3D MC1024 Cabinet 0



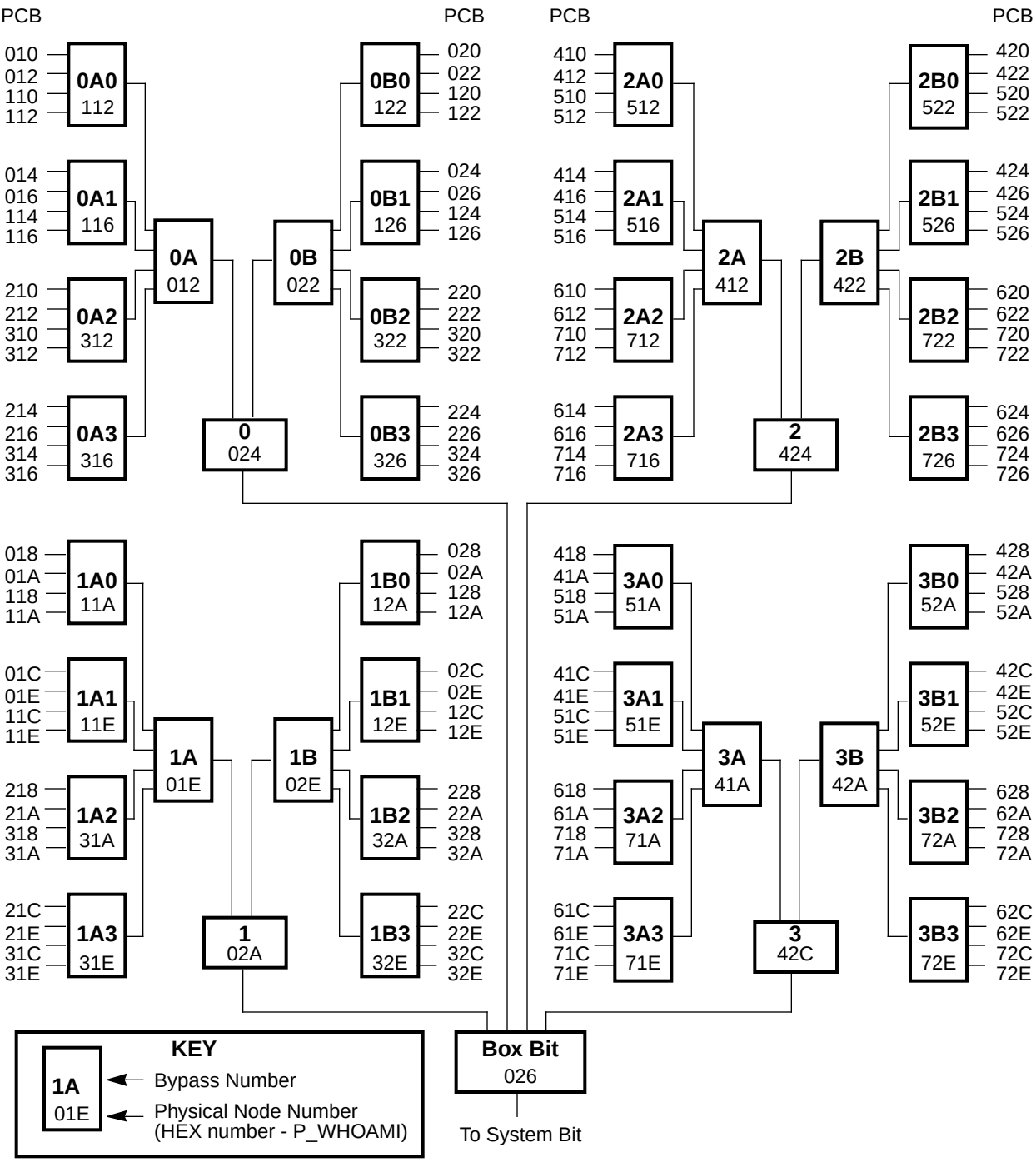
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 51. Barrier Synchronization Circuit 2 in CRAY T3D MC1024 Cabinet 1



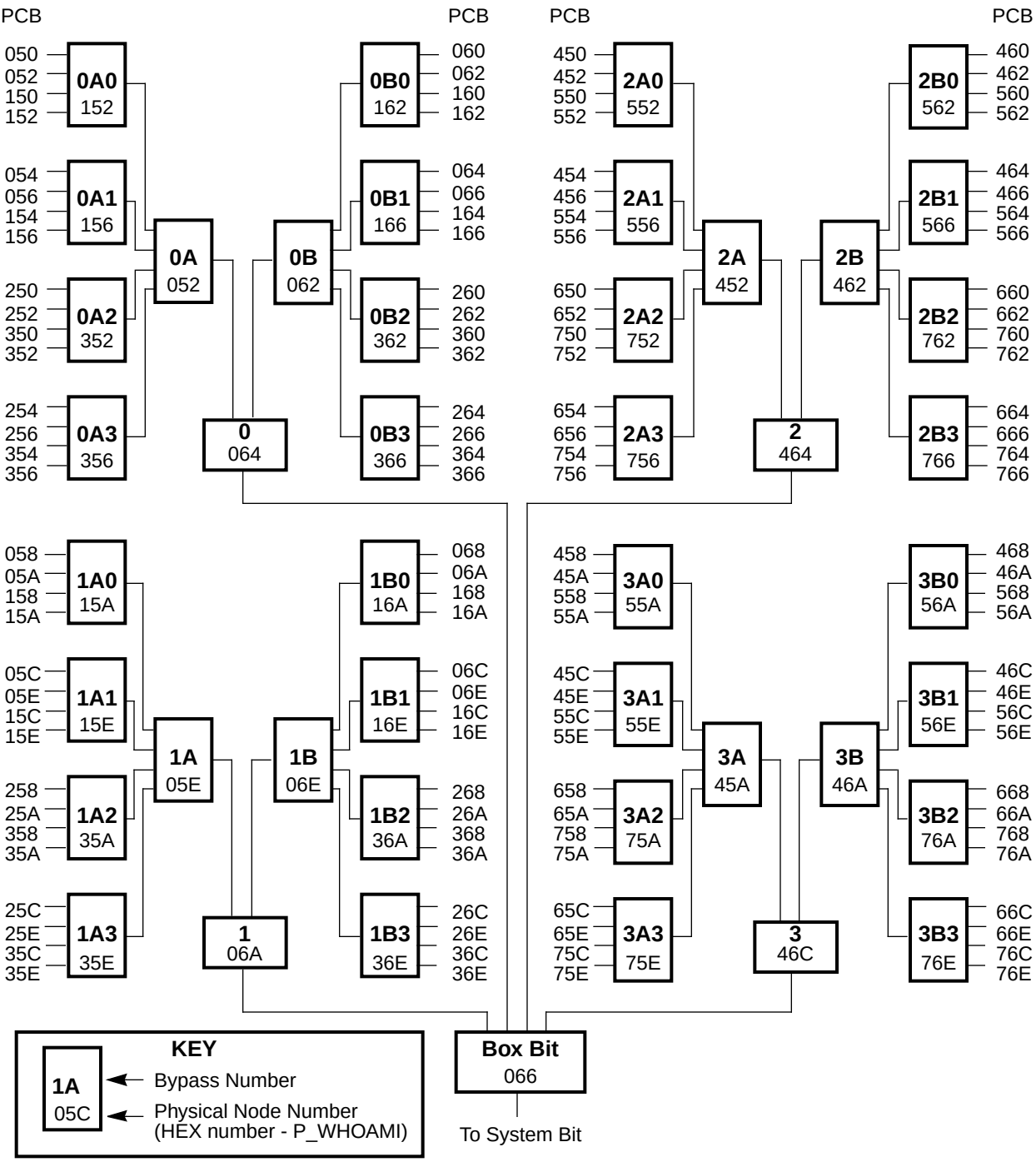
NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 52. Barrier Synchronization Circuit 2 CRAY T3D MC1024 System Bit



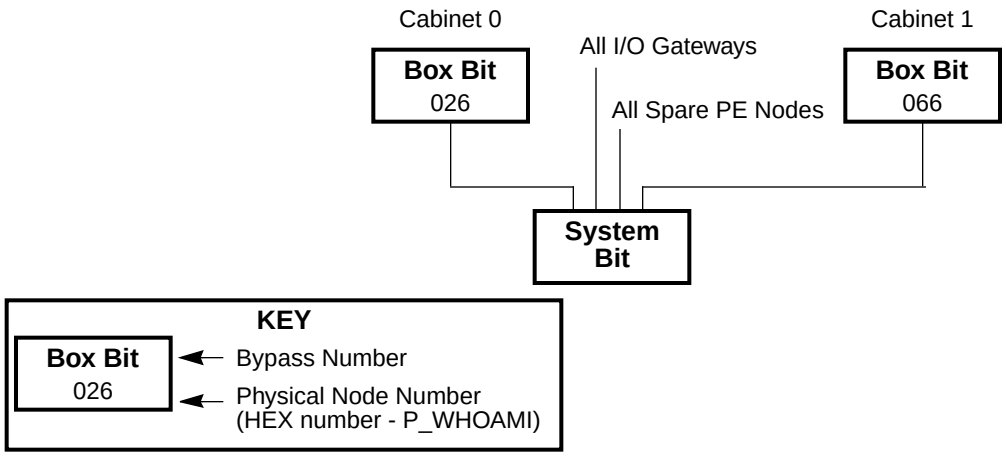
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 53. Barrier Synchronization Circuit 3 in CRAY T3D MC1024 Cabinet 0



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 54. Barrier Synchronization Circuit 3 in CRAY T3D MC1024 Cabinet 1



NOTE: The bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 55. Barrier Synchronization Circuit 3 CRAY T3D MC1024 System Bit

4 CRAY T3D MC512 System

The CRAY T3D MC512 system contains 512 PEs in 256 processing element nodes and is housed in one cabinet. The following subsections describe the communication links, module layout, and barrier synchronization bypass points for the CRAY T3D MC512 system.

NOTE: Throughout this document, physical PE numbers are represented as three-digit hexadecimal numbers that correspond to the physical PE numbers in the P_WHOAMI registers. For example, a PE may have a physical PE number of $10B_{16}$.

NOTE: Throughout this document, physical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $10A_{16}$ contains the physical PEs $10A_{16}$ and $10B_{16}$.

NOTE: Throughout this document, logical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a L_WHOAMI register with bit 2^0 set to 0. For example, logical node $10A_{16}$ contains the logical PEs $10A_{16}$ and $10B_{16}$.

4.1 CRAY T3D MC512 Communication Links

Figure 56 shows the physical communication links between nodes in the Y dimension.

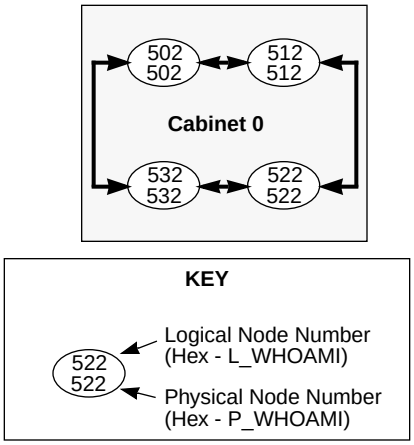


Figure 56. CRAY T3D MC512 Y-dimension Communication Links

Figure 57 shows the physical communication links between spare nodes in the Y dimension.

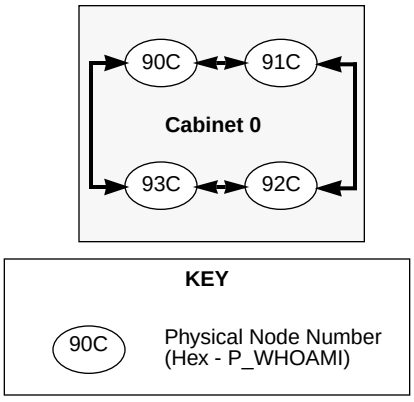


Figure 57. CRAY T3D MC512 Spare Node Y-dimension Communication Links

Figure 58 shows the physical communication links between the nodes in the X and Z dimensions. For clarity the figures do not show the communication links that complete the torus in the X and Z dimension.

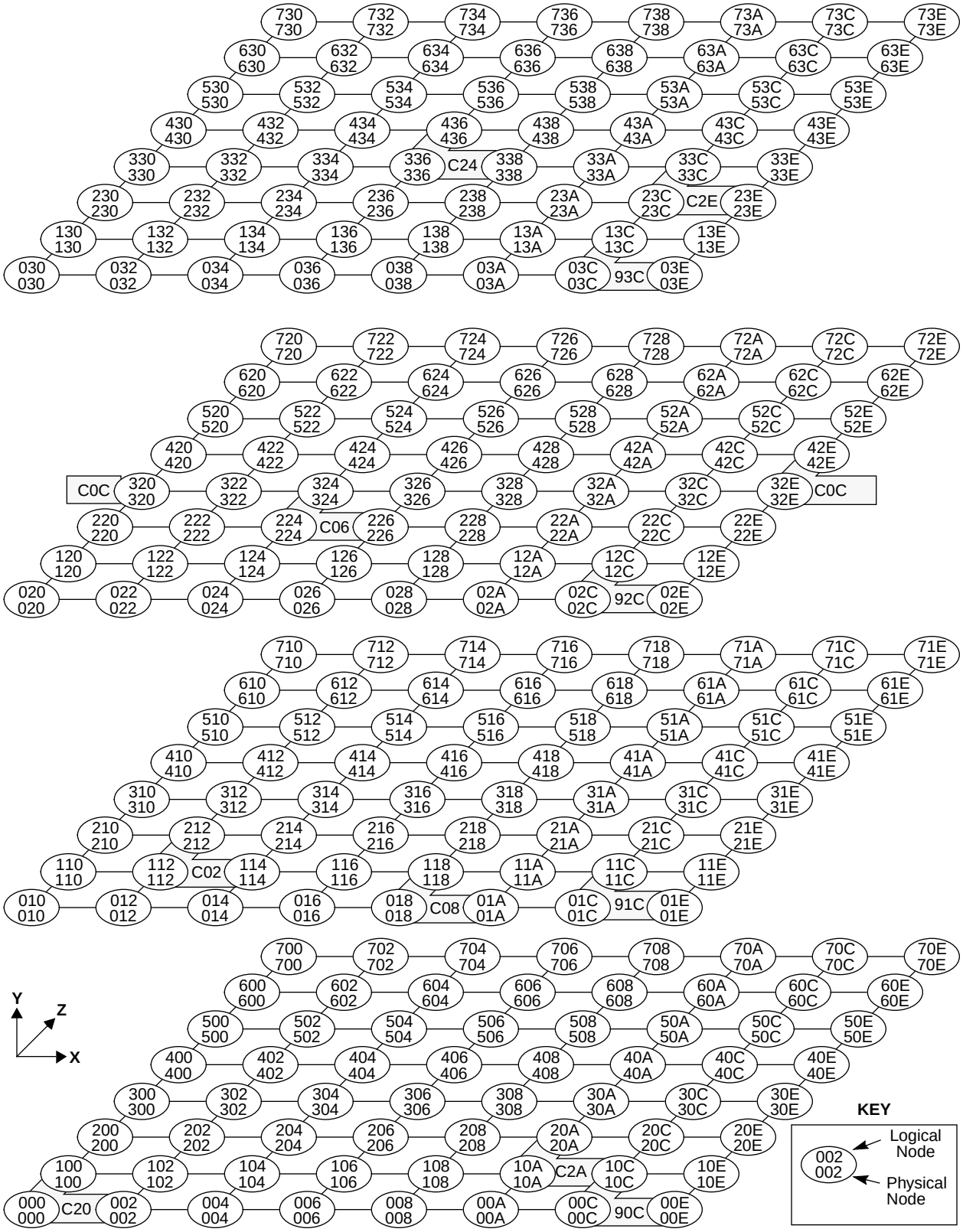


Figure 58. CRAY T3D MC512 X- and Z-dimension Communication Links

4.2 CRAY T3D MC512 Module Layout

Figure 59 shows the module layout and physical node locations in the CRAY T3D MC512 system cabinet. Each figure represents the physical node number as a three-digit hexadecimal number that is equivalent to the number read from the P_WHOAMI register with bit 2^0 set to 0. For example, physical node 002_{16} contains the physical PEs 002_{16} and 003_{16}.

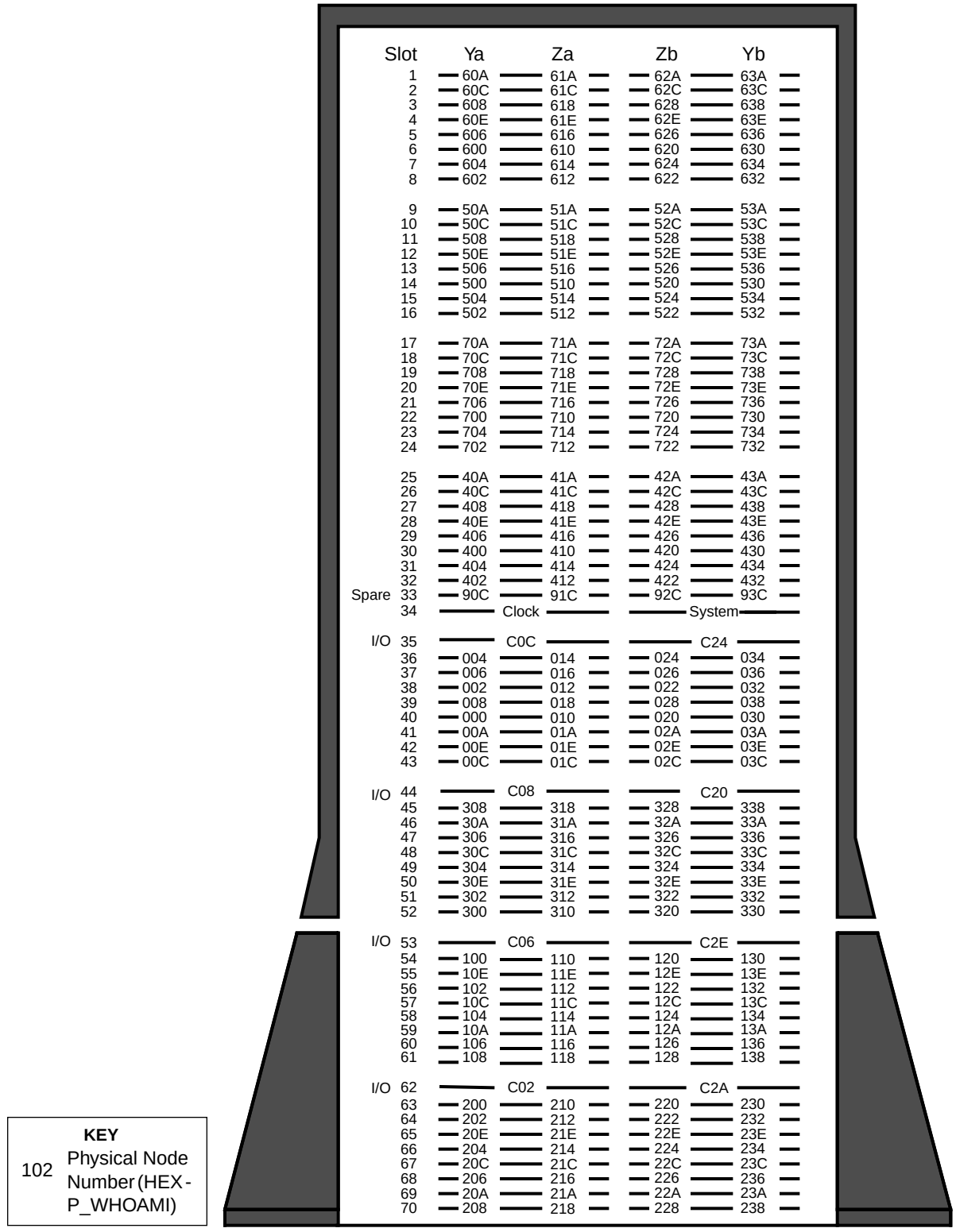


Figure 59. CRAY T3D MC512 Module Layout

4.3 CRAY T3D MC512 Barrier Synchronization Circuits

Figure 60 through Figure 63 show the barrier synchronization bypass points for all four physical barrier synchronization circuits in the CRAY T3D MC512 system. In these figures, the printed circuit board (PCB) bypass points and all other bypass points are shown.

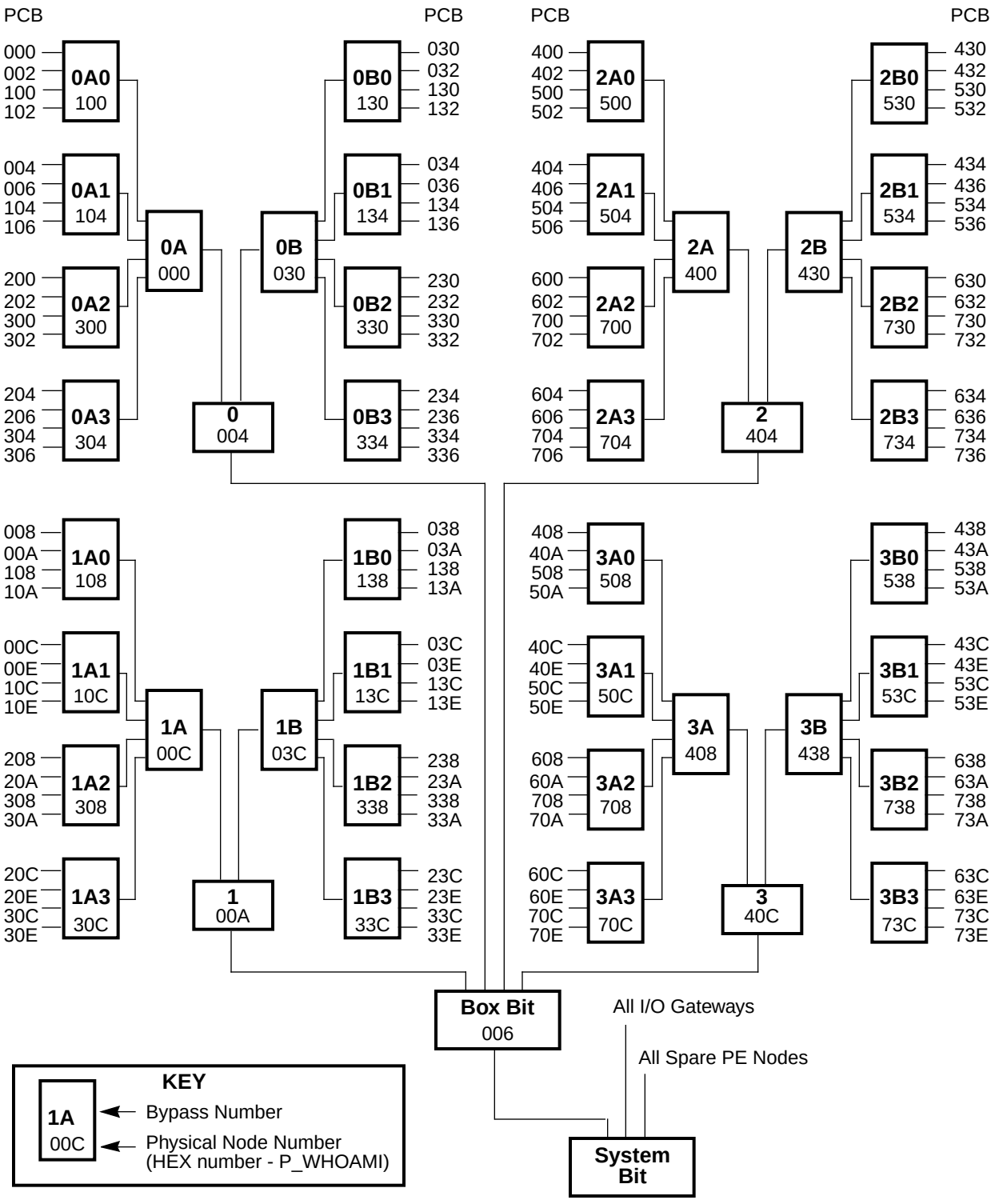
The PCB bypass points are controlled by bit 2^{11} or bit 2^{12} of the network mode register (NODE_CSR). Every processing element node PCB contains four PCB bypass points (one for each physical barrier synchronization circuit).

Each PCB bypass point is given a name that corresponds to the physical node that controls the bypass point. For example, the PCB bypass point 402 in barrier synchronization circuit 0 is located on the PCB that contains physical PEs 402_{16}, 403_{16}, 412_{16}, and 413_{16}. This bypass is controlled by setting bit 2^{11} of the NODE_CSR in physical node 402 (which contains physical PEs 402_{16} and 403_{16}) to the appropriate value.

When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 0, the output of the AND gate in a PCB bypass point is redirected to the fanout block in the bypass point. When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 1, the output of the AND gate in a PCB bypass point is directed to a second-level bypass point.

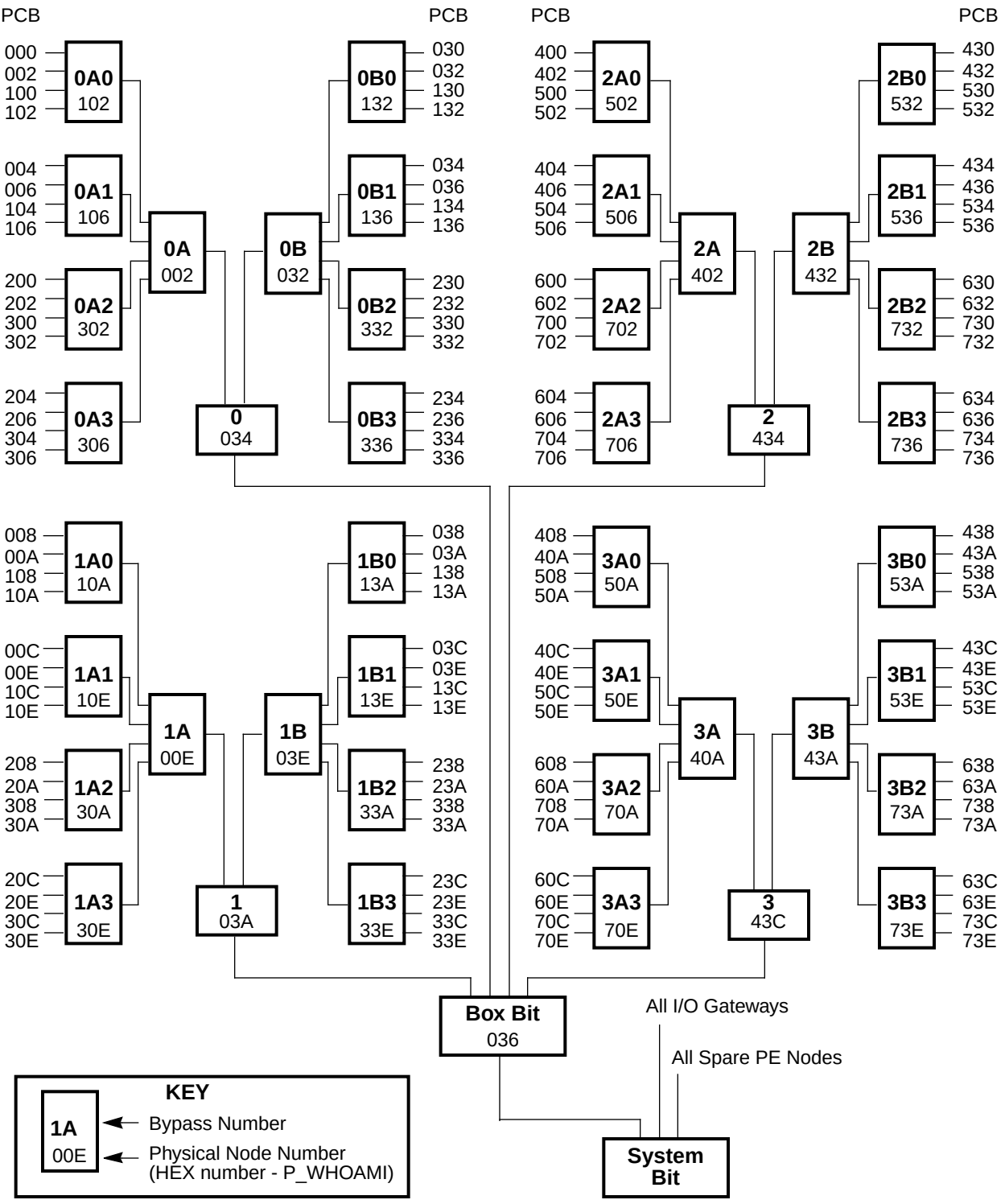
The other bypass points shown in the following figures are controlled by bit 2^{13} of the NODE_CSR. For example, bypass point 0A in barrier synchronization circuit 0 of cabinet 0 is controlled by setting bit 2^{13} of the NODE_CSR in physical node 000_{16} (which contains physical PEs 000_{16} and 001_{16}) to the appropriate value.

When bit 2^{13} of the NODE_CSR is set to 0, the output of the AND gate in the bypass point is redirected to the fanout block in the bypass point. When bit 2^{13} of the NODE_CSR is set to 1, the output of the AND gate in the bypass point is directed to the next-level bypass point.



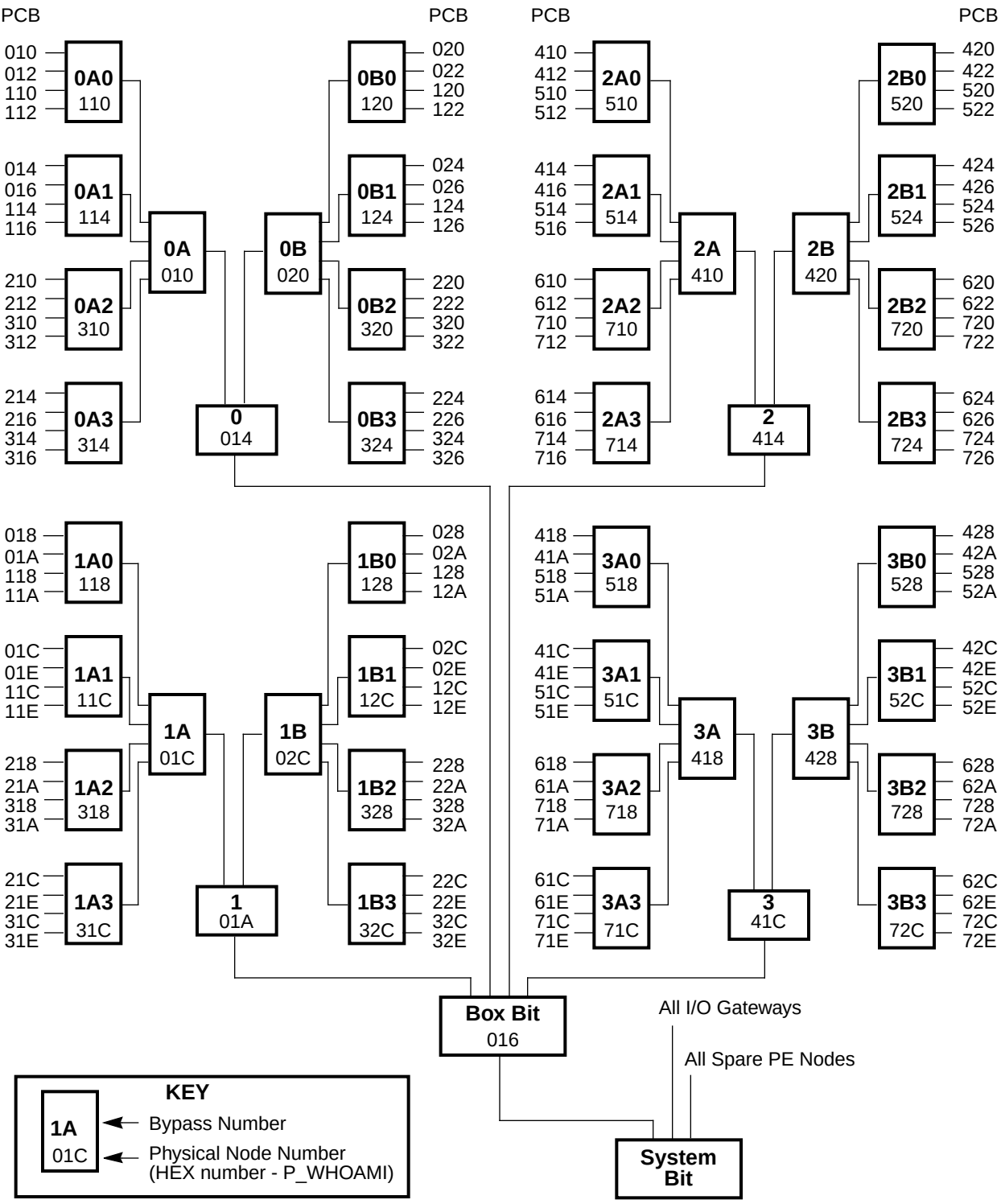
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 60. Barrier Synchronization Circuit 0 in CRAY T3D MC512 System



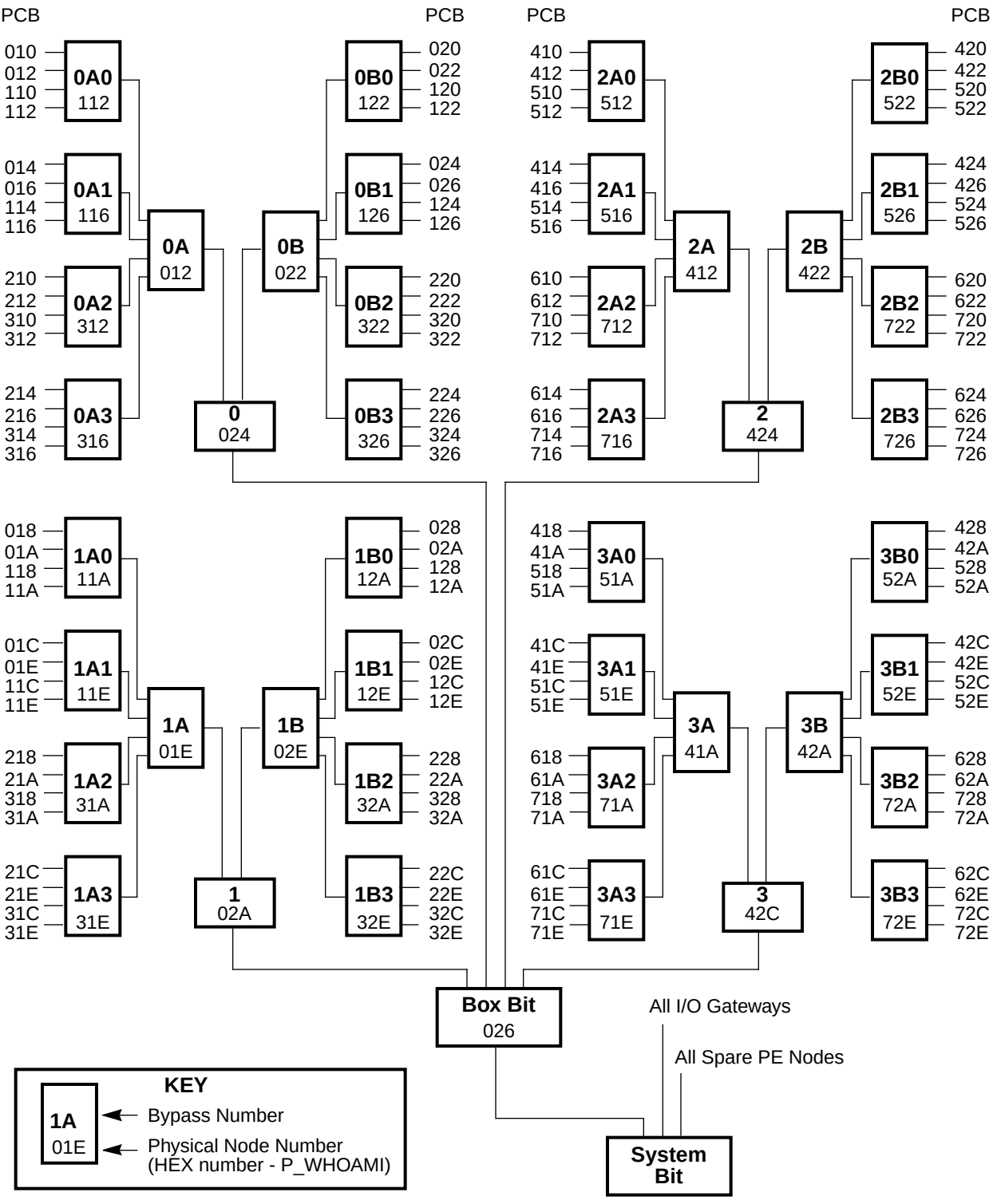
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 61. Barrier Synchronization Circuit 1 in CRAY T3D MC512 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 62. Barrier Synchronization Circuit 2 in CRAY T3D MC512



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 63. Barrier Synchronization Circuit 3 in CRAY T3D MC512 System

5 CRAY T3D MC256 System

The CRAY T3D MC256 system contains 256 PEs in 128 processing element nodes and is housed in one cabinet. The following subsections describe the communication links, module layout, and barrier synchronization bypass points for the CRAY T3D MC256 system.

NOTE: Throughout this document, physical PE numbers are represented as three-digit hexadecimal numbers that correspond to the physical PE numbers in the P_WHOAMI registers. For example, a PE may have a physical PE number of $10B_{16}$.

NOTE: Throughout this document, physical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $10A_{16}$ contains the physical PEs $10A_{16}$ and $10B_{16}$.

NOTE: Throughout this document, logical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a L_WHOAMI register with bit 2^0 set to 0. For example, logical node $10A_{16}$ contains the logical PEs $10A_{16}$ and $10B_{16}$.

5.1 CRAY T3D MC256 Communication Links

Figure 64 shows the physical communication links between nodes in the Y dimension.

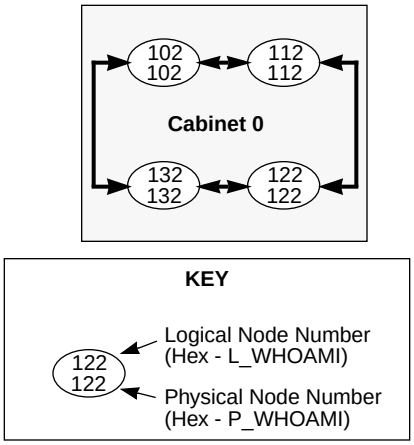


Figure 64. CRAY T3D MC256 Y-dimension Communication Links

Figure 65 shows the physical communication links between spare nodes in the Y dimension.

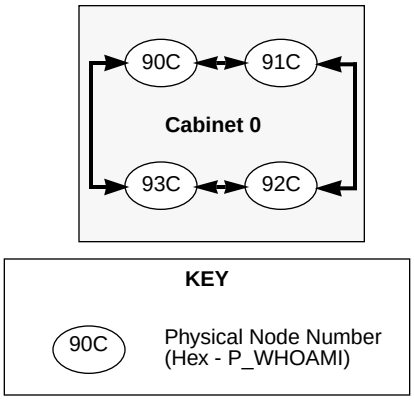


Figure 65. CRAY T3D MC256 Spare Node Y-dimension Communication Links

Figure 66 shows the physical communication links between the nodes in the X and Z dimensions. For clarity the figures do not show the communication links that complete the torus in the X and Z dimensions.

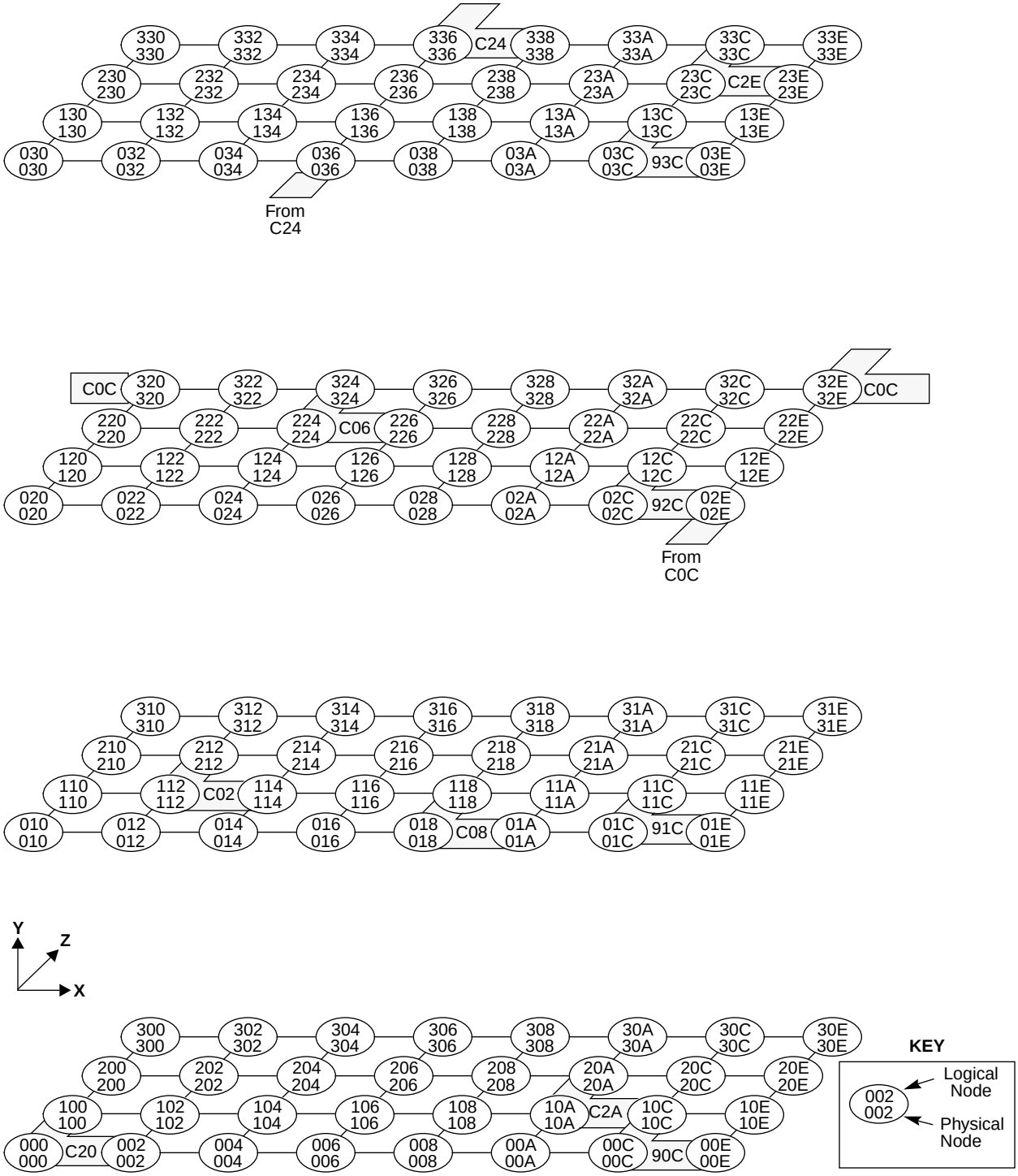


Figure 66. CRAY T3D MC256 X- and Z-dimension Communication Links

5.2 CRAY T3D MC256 Module Layout

Figure 67 shows the module layout and physical node locations in the CRAY T3D MC256 system cabinet. Each figure represents the physical node number as a three-digit hexadecimal number that is equivalent to the number read from the P_WHOAMI register with bit 2^0 set to 0. For example, physical node 002_{16} contains the physical PEs 002_{16} and 003_{16}.

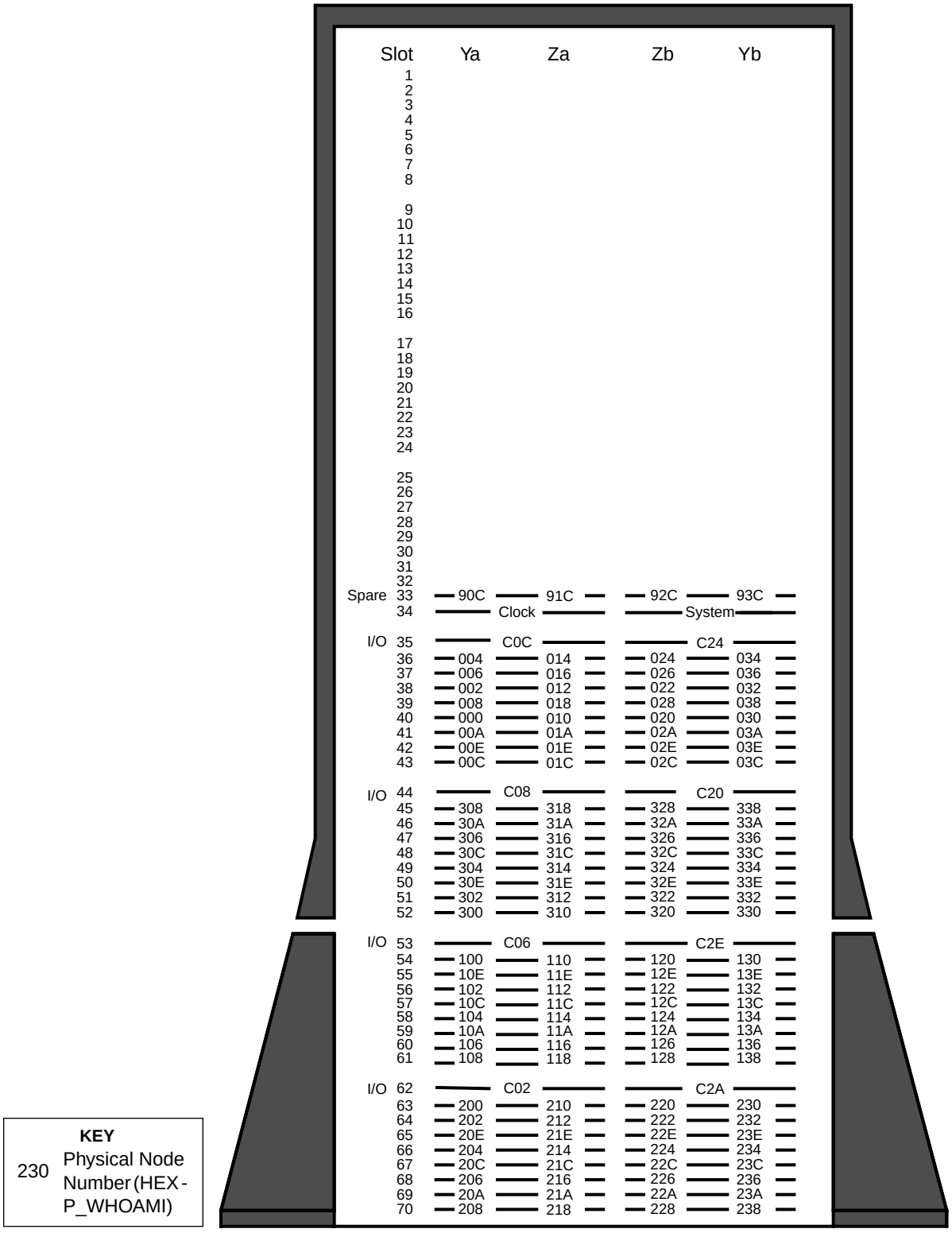


Figure 67. CRAY T3D MC256 Module Layout

5.3 CRAY T3D MC256 Barrier Synchronization Circuits

Figure 68 through Figure 71 show the barrier synchronization bypass points for all four physical barrier synchronization circuits in the CRAY T3D MC256 system. In these figures, the printed circuit board (PCB) bypass points and all other bypass points are shown.

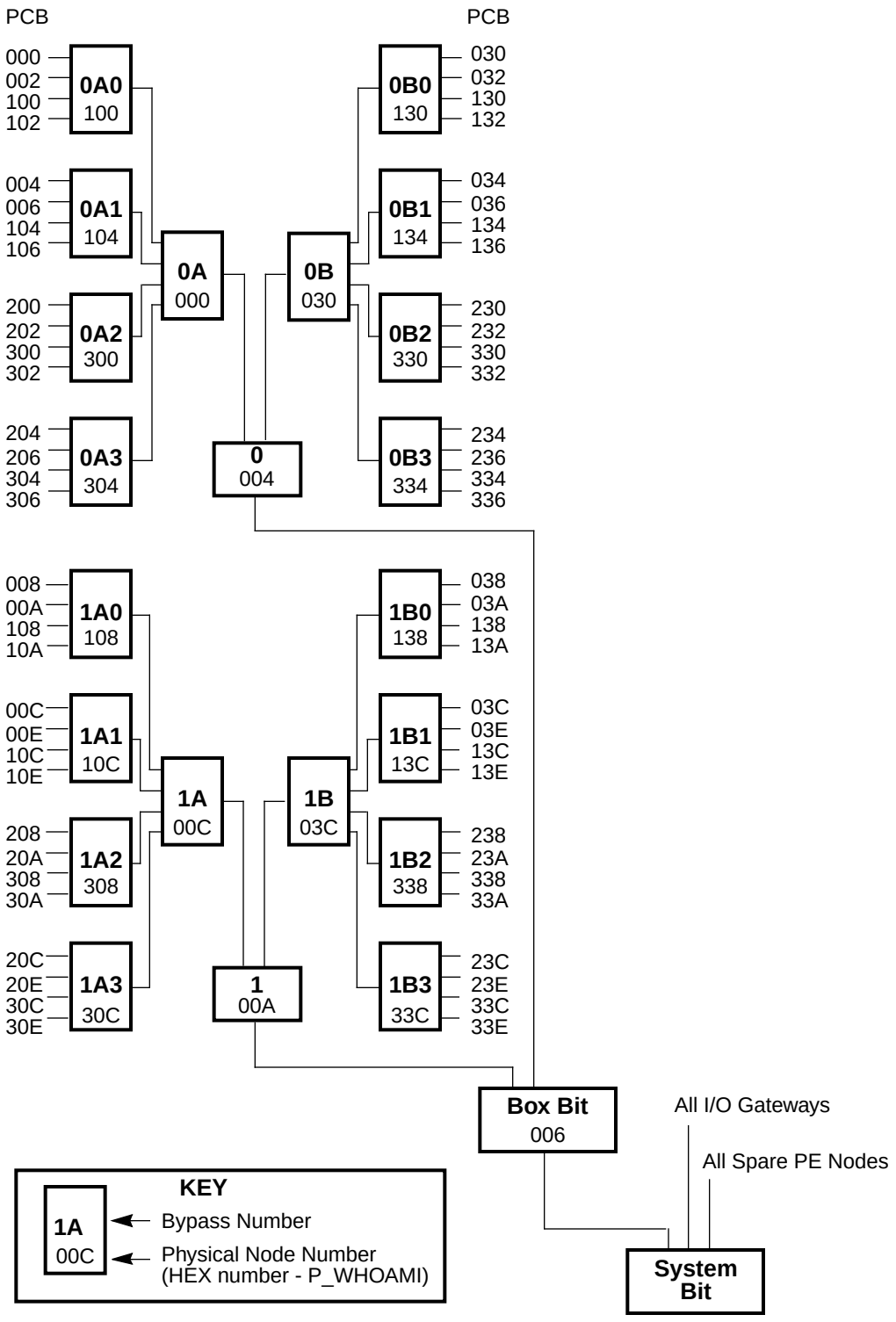
The PCB bypass points are controlled by bit 2^{11} or bit 2^{12} of the network mode register (NODE_CSR). Every processing element node PCB contains four PCB bypass points (one for each physical barrier synchronization circuit).

Each PCB bypass point is given a name that corresponds to the physical node that controls the bypass point. For example, the PCB bypass point 002 in barrier synchronization circuit 0 is located on the PCB that contains physical PEs 002_{16}, 003_{16}, 012_{16}, and 013_{16}. This bypass is controlled by setting bit 2^{11} of the NODE_CSR in physical node 002 (which contains physical PEs 002_{16} and 003_{16}) to the appropriate value.

When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 0, the output of the AND gate in a PCB bypass point is redirected to the fanout block in the bypass point. When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 1, the output of the AND gate in a PCB bypass point is directed to a second-level bypass point.

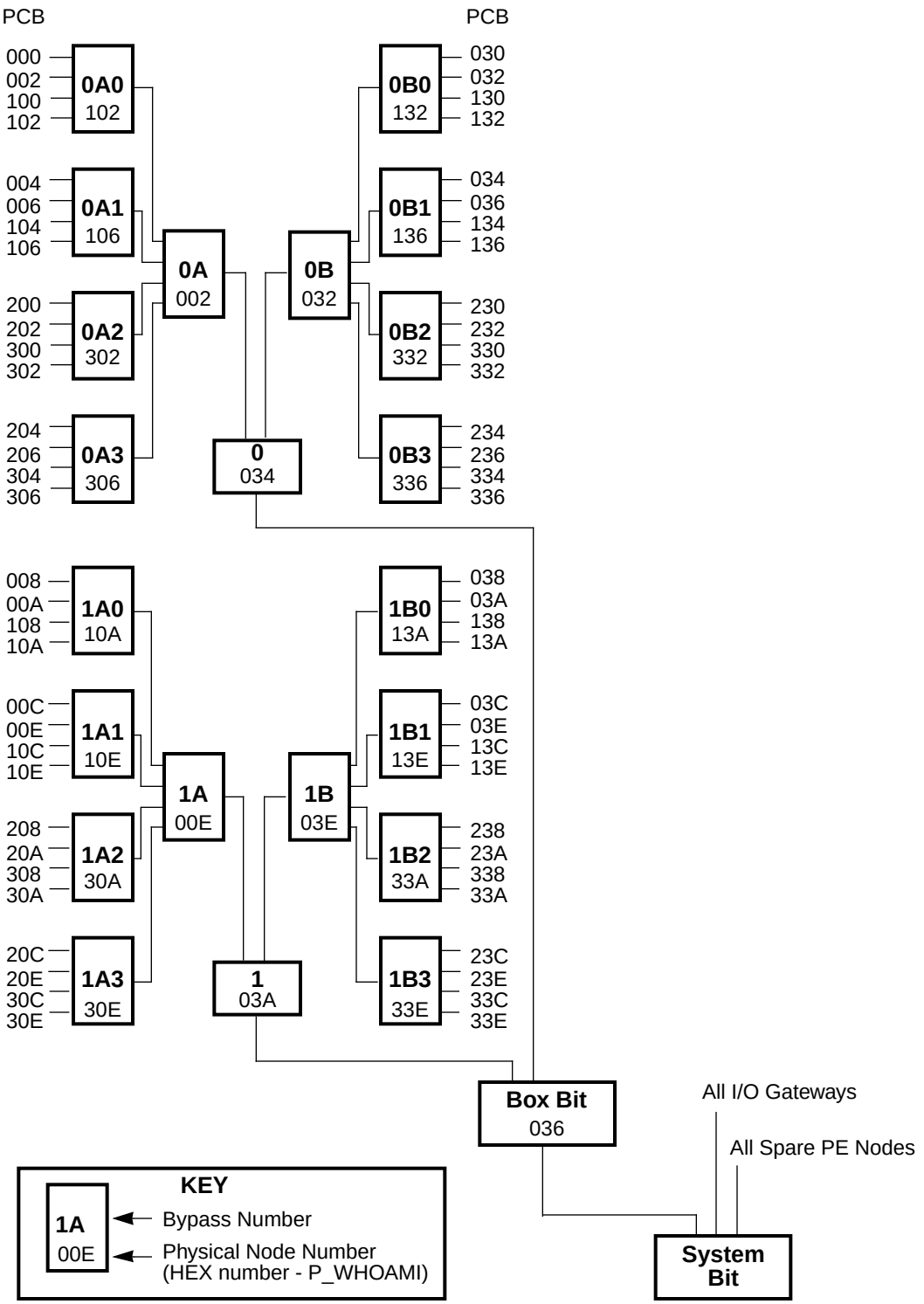
The other bypass points shown in the following figures are controlled by bit 2^{13} of the NODE_CSR. For example, bypass point 0A in barrier synchronization circuit 0 of cabinet 0 is controlled by setting bit 2^{13} of the NODE_CSR in physical node 000_{16} (which contains physical PEs 000_{16} and 001_{16}) to the appropriate value.

When bit 2^{13} of the NODE_CSR is set to 0, the output of the AND gate in the bypass point is redirected to the fanout block in the bypass point. When bit 2^{13} of the NODE_CSR is set to 1, the output of the AND gate in the bypass point is directed to the next-level bypass point.



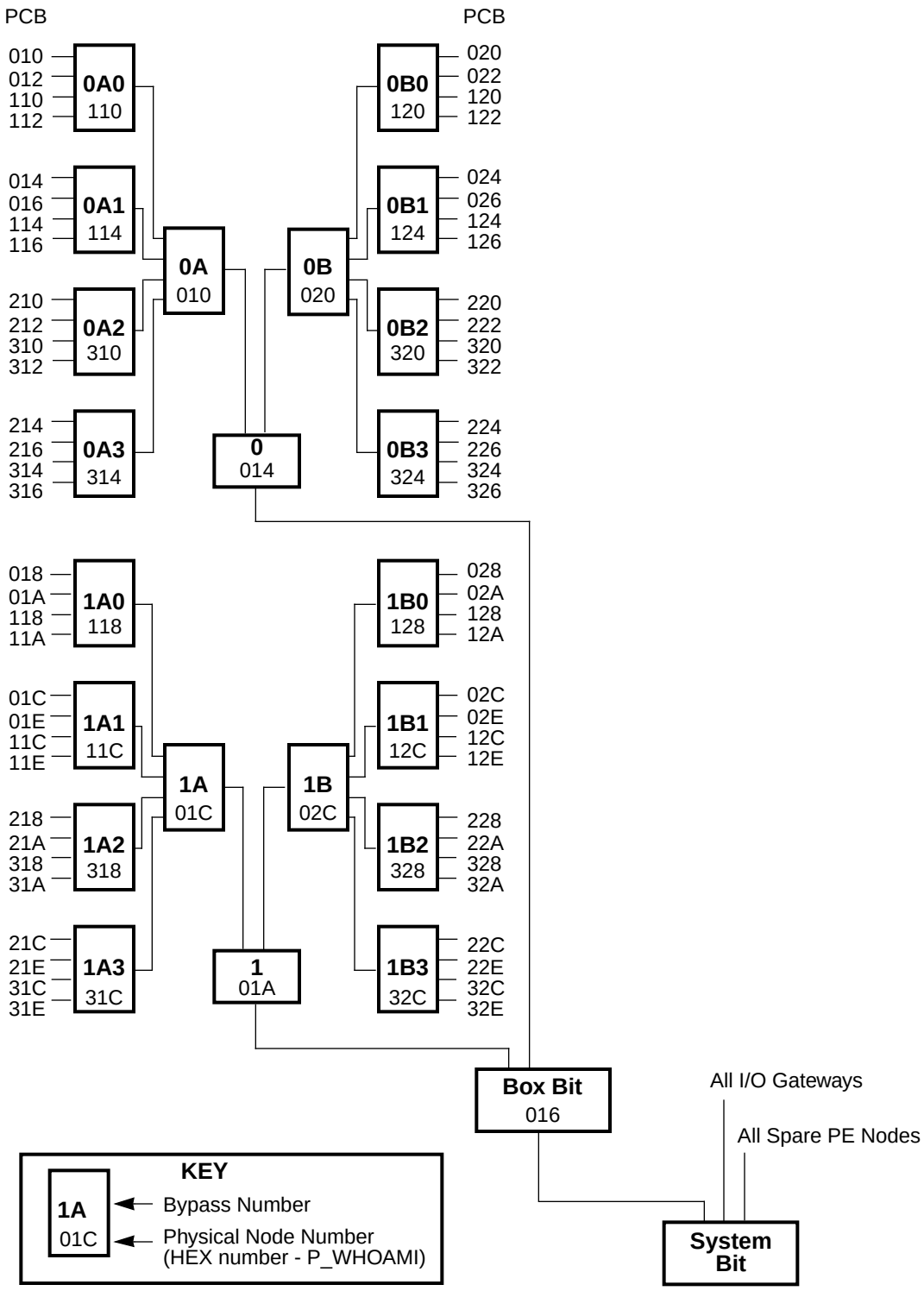
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 68. Barrier Synchronization Circuit 0 in CRAY T3D MC256 System



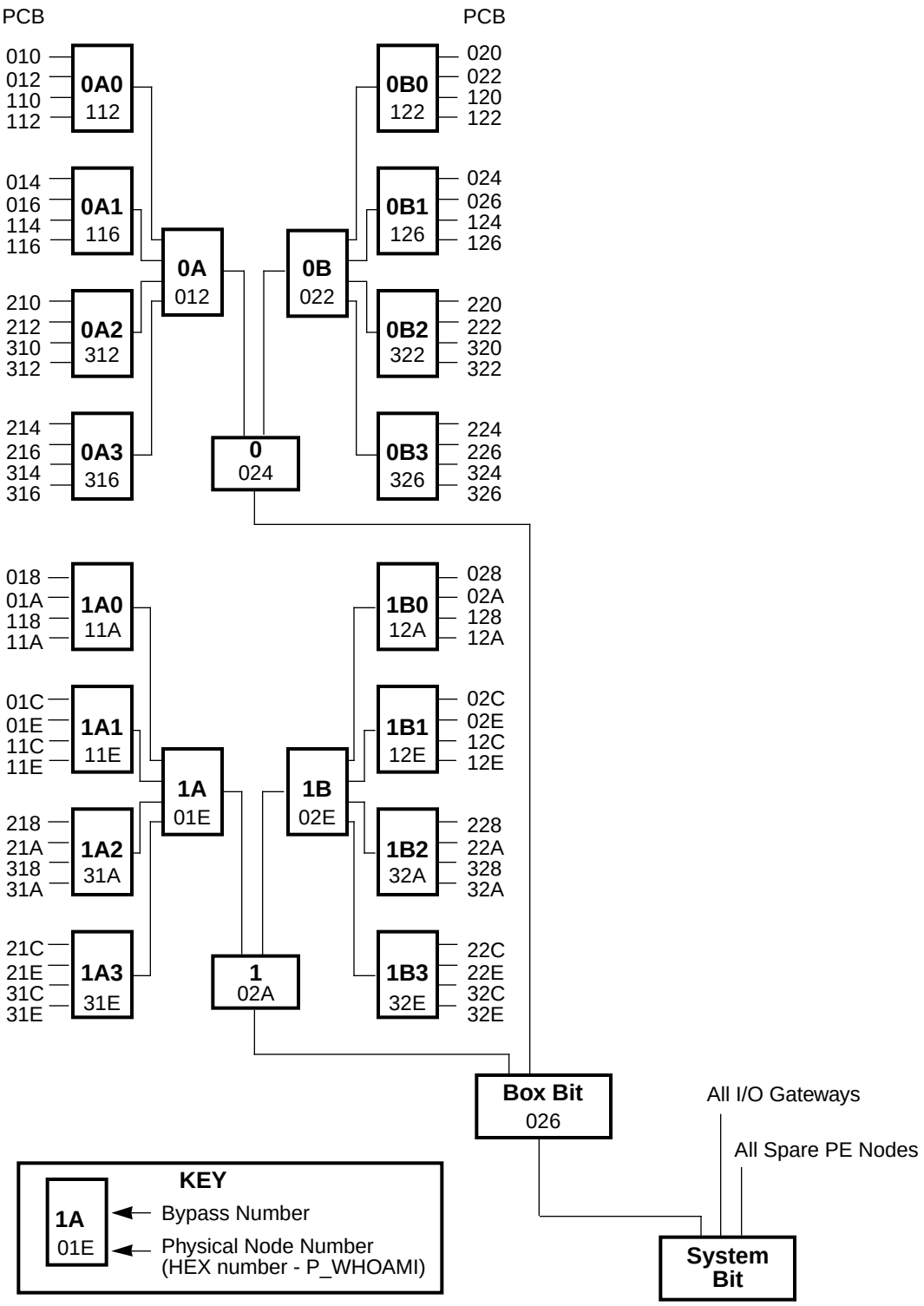
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 69. Barrier Synchronization Circuit 1 in CRAY T3D MC256 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 70. Barrier Synchronization Circuit 2 in CRAY T3D MC256 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 71. Barrier Synchronization Circuit 3 in CRAY T3D MC256 System

6 CRAY T3D MC128 System

The CRAY T3D MC128 system contains 128 PEs in 64 processing element nodes and is housed in one cabinet. The following subsections describe the communication links, module layout, and barrier synchronization bypass points for the CRAY T3D MC128 system.

NOTE: Throughout this document, physical PE numbers are represented as three-digit hexadecimal numbers that correspond to the physical PE numbers in the P_WHOAMI registers. For example, a PE may have a physical PE number of $10B_{16}$.

NOTE: Throughout this document, physical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $10A_{16}$ contains the physical PEs $10A_{16}$ and $10B_{16}$.

NOTE: Throughout this document, logical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a L_WHOAMI register with bit 2^0 set to 0. For example, logical node $10A_{16}$ contains the logical PEs $10A_{16}$ and $10B_{16}$.

6.1 CRAY T3D MC128 Communication Links

Figure 72 shows the physical communication links between nodes in the Y dimension.

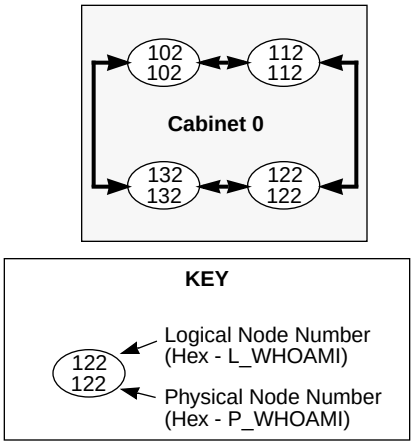


Figure 72. CRAY T3D MC128 Y-dimension Communication Links

Figure 73 shows the physical communication links between spare nodes in the Y dimension.

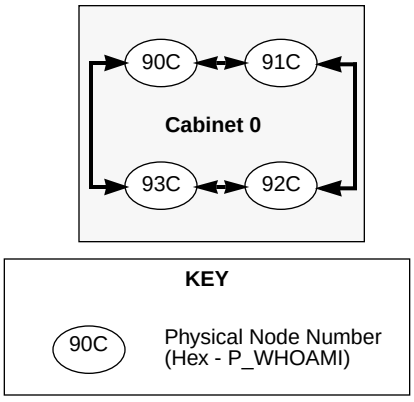


Figure 73. CRAY T3D MC128 Spare Node Y-dimension Communication Links

Figure 74 shows the physical communication links between the nodes in the X and Z dimensions. For clarity the figure does not show the communication links that complete the torus in the X and Z dimensions.

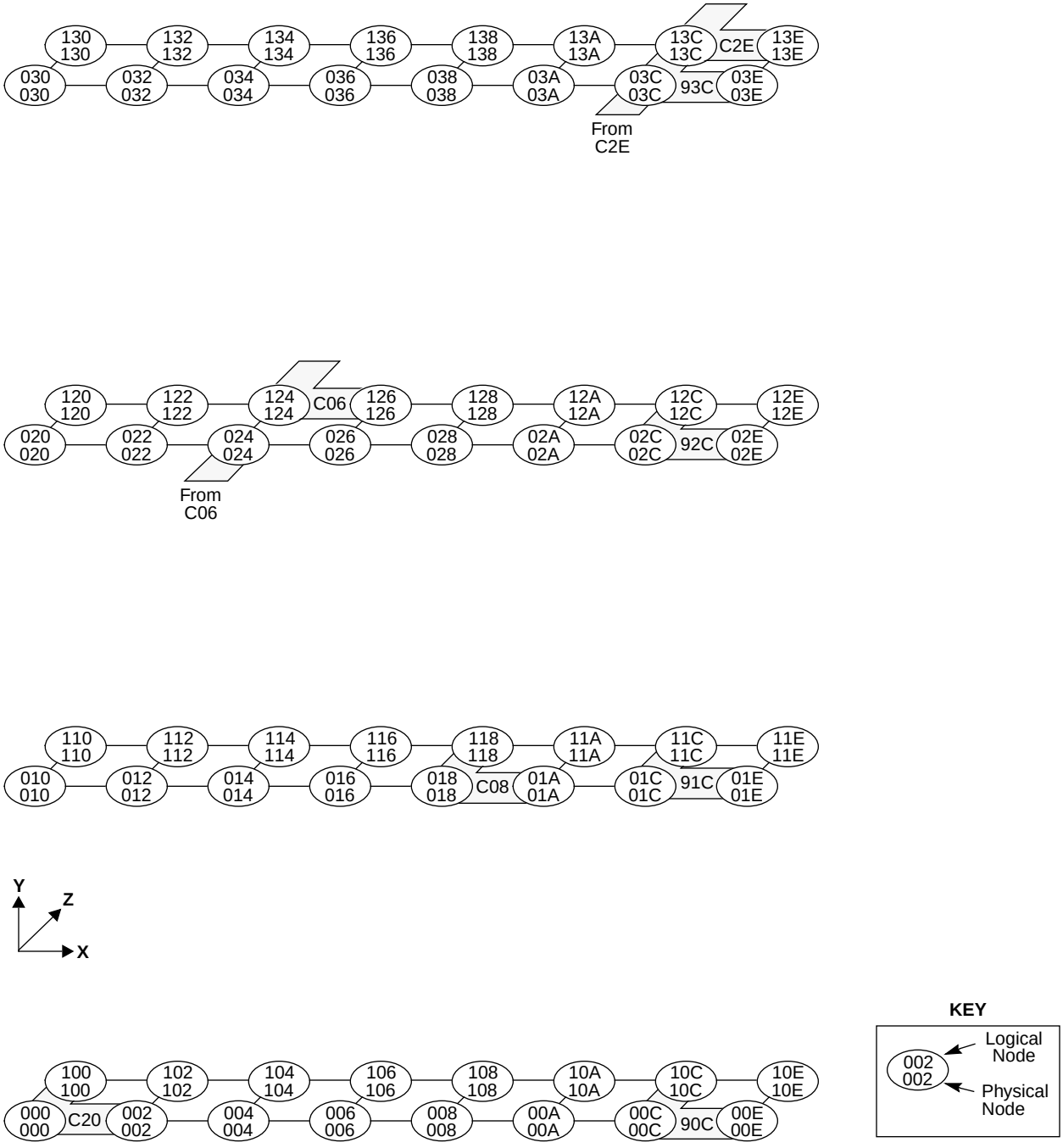


Figure 74. CRAY T3D MC128 X- and Z-dimension Communication Links

NOTE: The I/O Gateways C06 and C2E are do not connect to the same nodes in a CRAY T3D MC128 system as they do in a CRAY T3D MC256 or CRAY T3D MC512 system.

6.2 CRAY T3D MC128 Module Layout

Figure 75 shows the module layout and physical node locations in the CRAY T3D MC128 system cabinet. Each figure represents the physical node number as a three-digit hexadecimal number that is equivalent to the number read from the P_WHOAMI register with bit 2^0 set to 0. For example, physical node 002_{16} contains the physical PEs 002_{16} and 003_{16}.

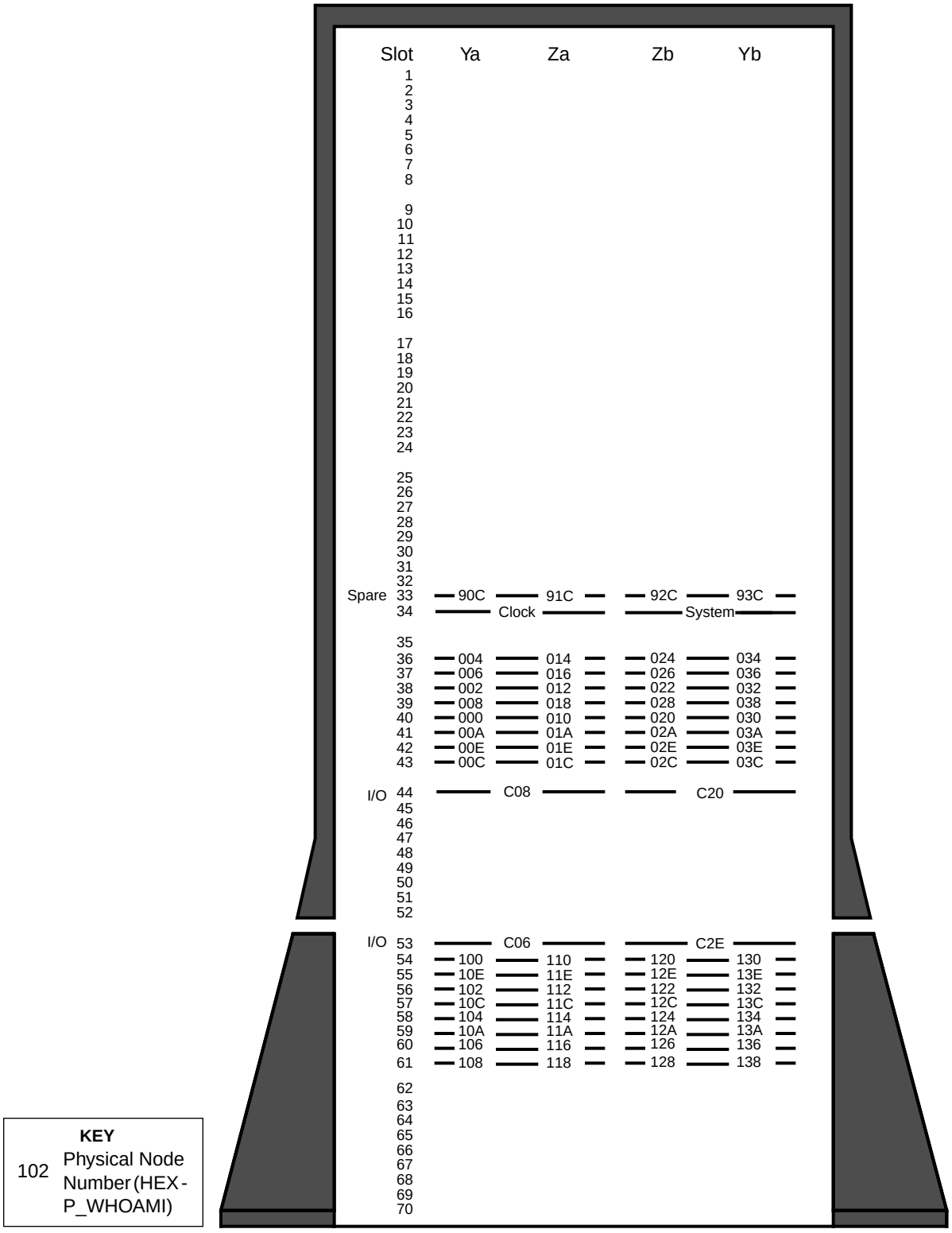


Figure 75. CRAY T3D MC128 Module Layout

6.3 CRAY T3D MC128 Barrier Synchronization Circuits

Figure 76 through Figure 79 show the barrier synchronization bypass points for all four physical barrier synchronization circuits in the CRAY T3D MC128 system. In these figures, the printed circuit board (PCB) bypass points and all other bypass points are shown.

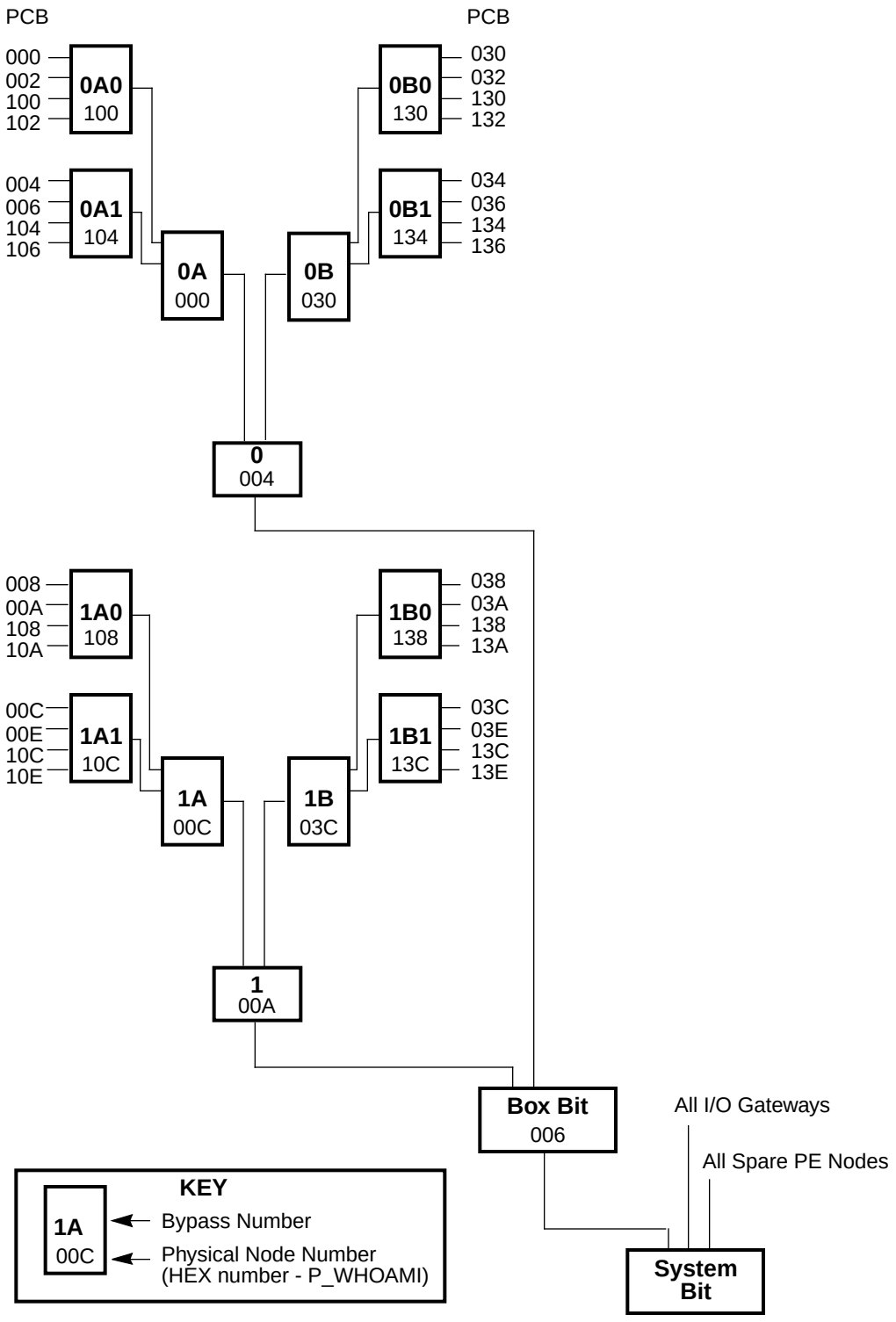
The PCB bypass points are controlled by bit 2^{11} or bit 2^{12} of the network mode register (NODE_CSR). Every processing element node PCB contains four PCB bypass points (one for each physical barrier synchronization circuit).

Each PCB bypass point is given a name that corresponds to the physical node that controls the bypass point. For example, the PCB bypass point 002 in barrier synchronization circuit 0 is located on the PCB that contains physical PEs 002_{16}, 003_{16}, 012_{16}, and 013_{16}. This bypass is controlled by setting bit 2^{11} of the NODE_CSR in physical node 002 (which contains physical PEs 002_{16} and 003_{16}) to the appropriate value.

When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 0, the output of the AND gate in a PCB bypass point is redirected to the fanout block in the bypass point. When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 1, the output of the AND gate in a PCB bypass point is directed to a second-level bypass point.

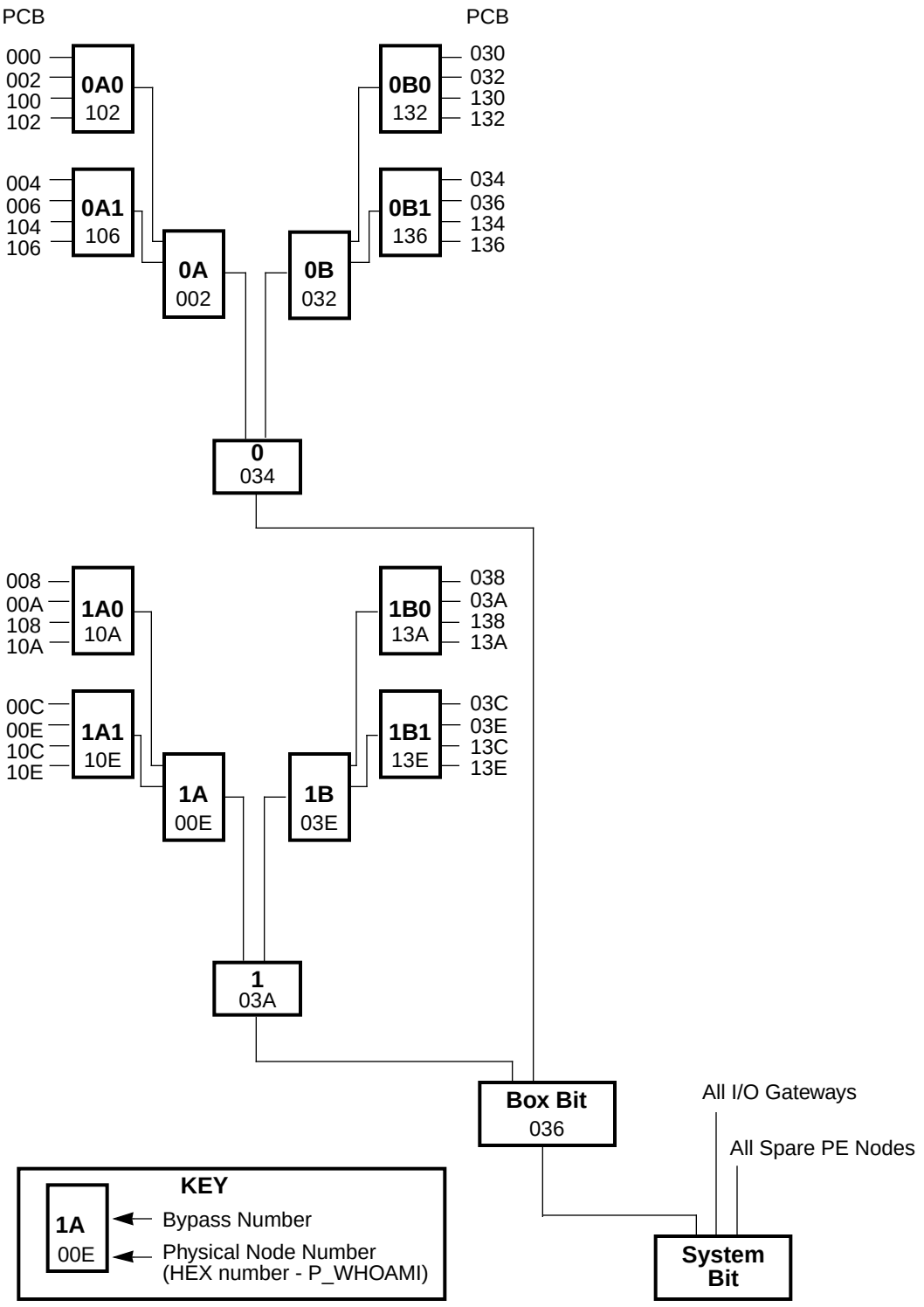
The other bypass points shown in the following figures are controlled by bit 2^{13} of the NODE_CSR. For example, bypass point 0A in barrier synchronization circuit 0 of cabinet 0 is controlled by setting bit 2^{13} of the NODE_CSR in physical node 000_{16} (which contains physical PEs 000_{16} and 001_{16}) to the appropriate value.

When bit 2^{13} of the NODE_CSR is set to 0, the output of the AND gate in the bypass point is redirected to the fanout block in the bypass point. When bit 2^{13} of the NODE_CSR is set to 1, the output of the AND gate in the bypass point is directed to the next-level bypass point.



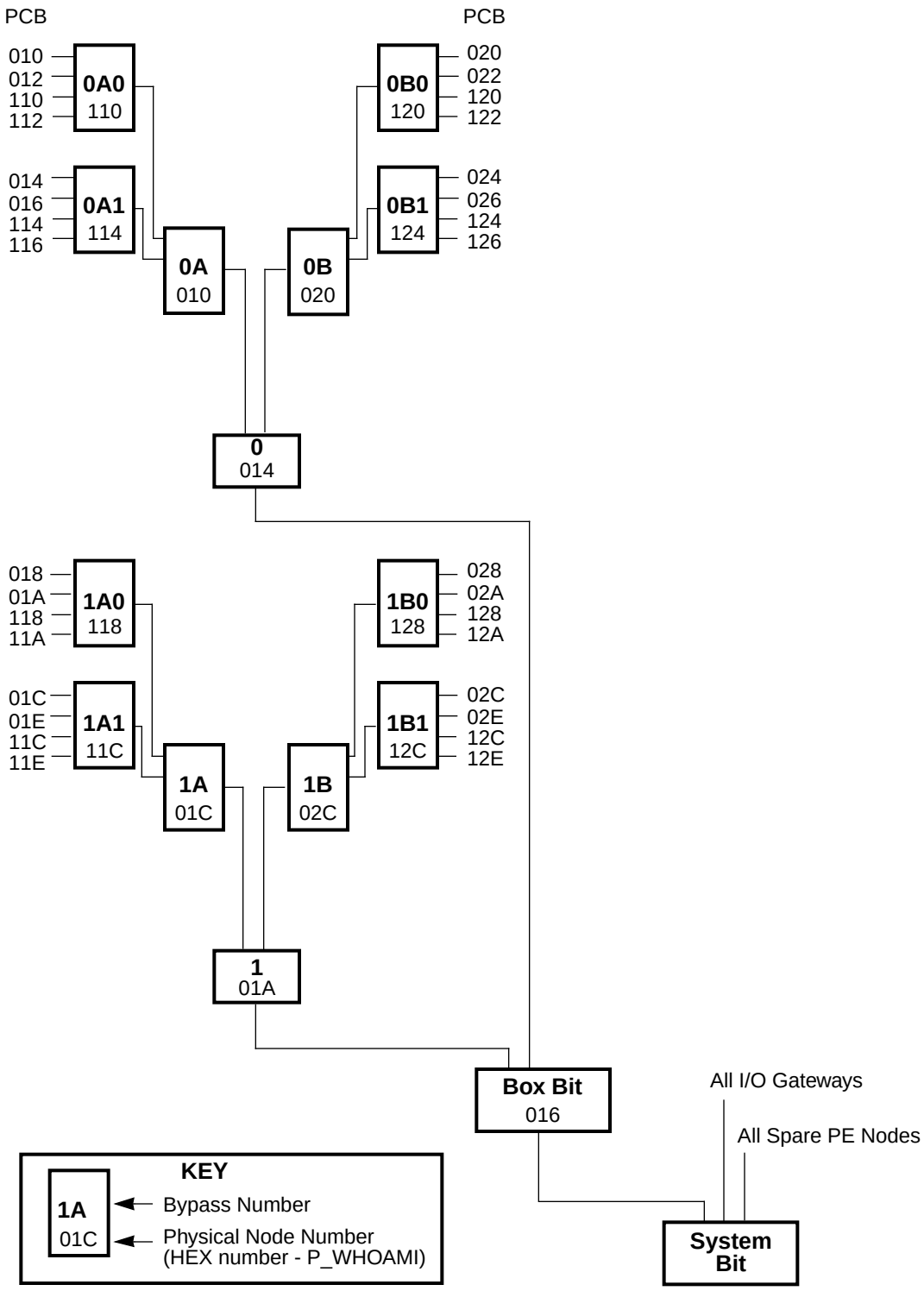
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 76. Barrier Synchronization Circuit 0 in CRAY T3D MC128 System



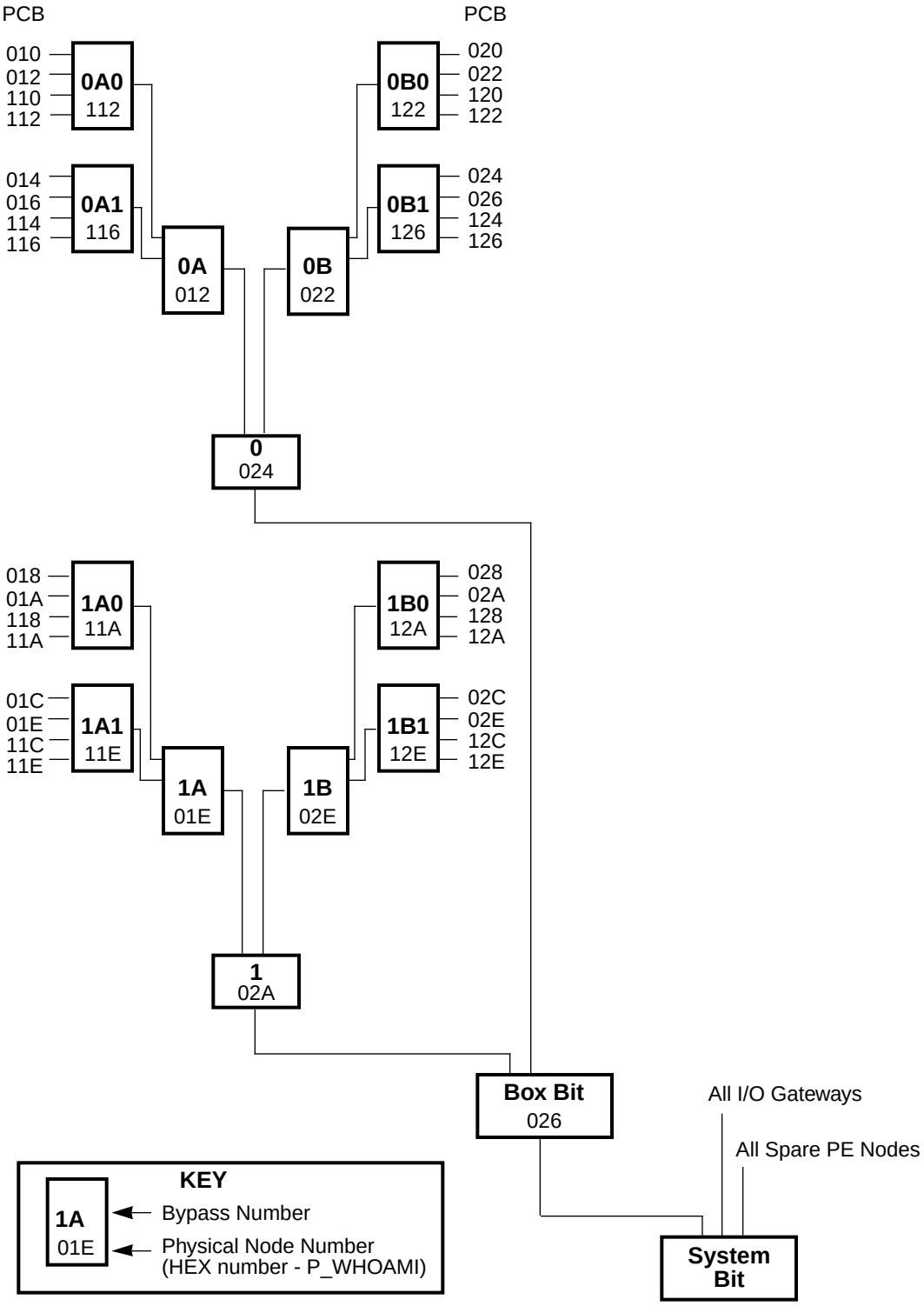
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 77. Barrier Synchronization Circuit 1 in CRAY T3D MC128 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 78. Barrier Synchronization Circuit 2 in CRAY T3D MC128 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 79. Barrier Synchronization Circuit 3 in CRAY T3D MC128 System

7 CRAY T3D MC64 System

The CRAY T3D MC64 system contains 64 PEs in 32 processing element nodes and is housed in one cabinet. The CRAY T3D MC64 system is only used in system test and check out (STCO).

The following subsections describe the communication links, module layout, and barrier synchronization bypass points for the CRAY T3D MC64 system.

NOTE: Throughout this document, physical PE numbers are represented as three-digit hexadecimal numbers that correspond to the physical PE numbers in the P_WHOAMI registers. For example, a PE may have a physical PE number of $10B_{16}$.

NOTE: Throughout this document, physical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $10A_{16}$ contains the physical PEs $10A_{16}$ and $10B_{16}$.

NOTE: Throughout this document, logical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a L_WHOAMI register with bit 2^0 set to 0. For example, logical node $10A_{16}$ contains the logical PEs $10A_{16}$ and $10B_{16}$.

7.1 CRAY T3D MC64 Communication Links

Figure 80 shows the physical communication links between nodes in the Y dimension.

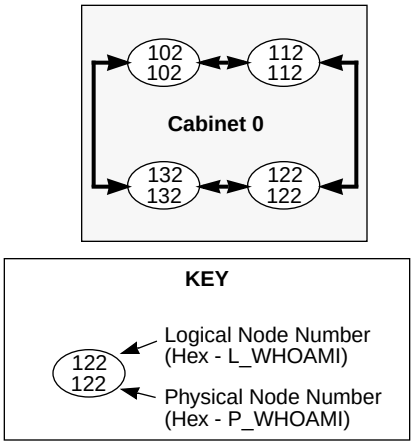


Figure 80. CRAY T3D MC64 Y-dimension Communication Links

Figure 81 shows the physical communication links between the nodes in the X and Z dimensions. For clarity the figure does not show the communication links that complete the torus in the X and Z dimensions.

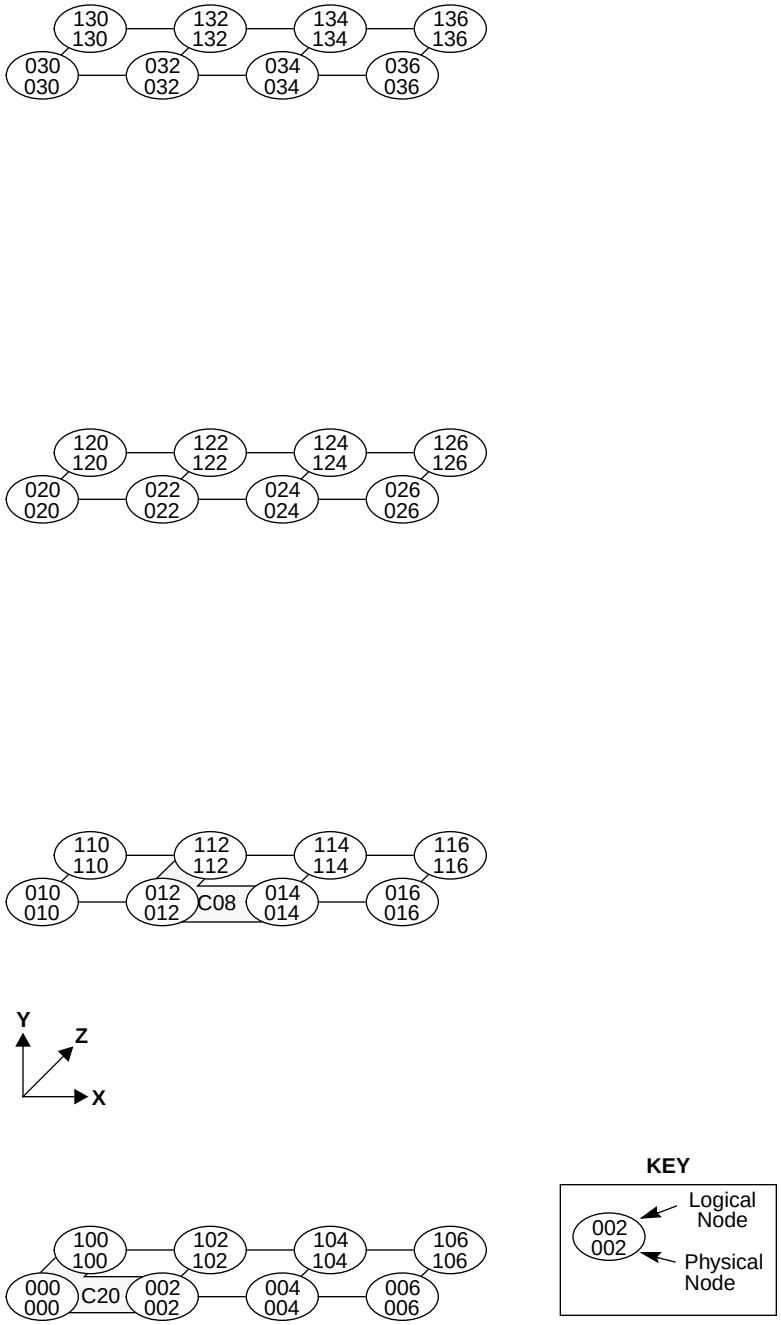


Figure 81. CRAY T3D MC64 X- and Z-dimension Communication Links

NOTE: The I/O Gateway C08 does not connect to the same nodes in a CRAY T3D MC64 system as it does in a CRAY T3D MC128 system.

7.2 CRAY T3D MC64 Module Layout

Figure 82 shows the module layout and physical node locations in the CRAY T3D MC64 system cabinet. Each figure represents the physical node number as a three-digit hexadecimal number that is equivalent to the number read from the P_WHOAMI register with bit 2^0 set to 0. For example, physical node 002_{16} contains the physical PEs 002_{16} and 003_{16}.

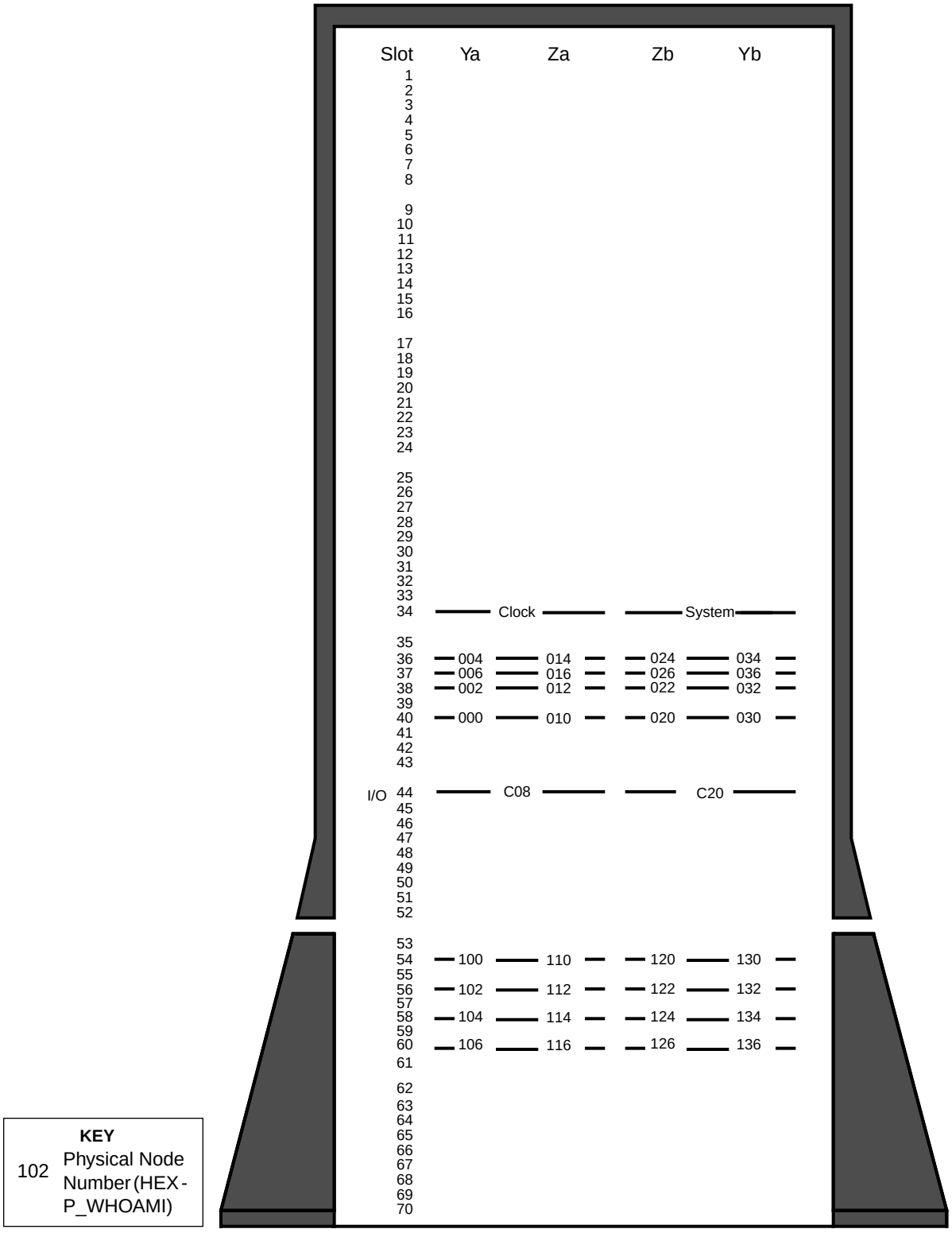


Figure 82. CRAY T3D MC64 Module Layout

7.3 CRAY T3D MC64 Barrier Synchronization Circuits

Figure 83 through Figure 86 show the barrier synchronization bypass points for all four physical barrier synchronization circuits in the CRAY T3D MC64 system. In these figures, the printed circuit board (PCB) bypass points and all other bypass points are shown.

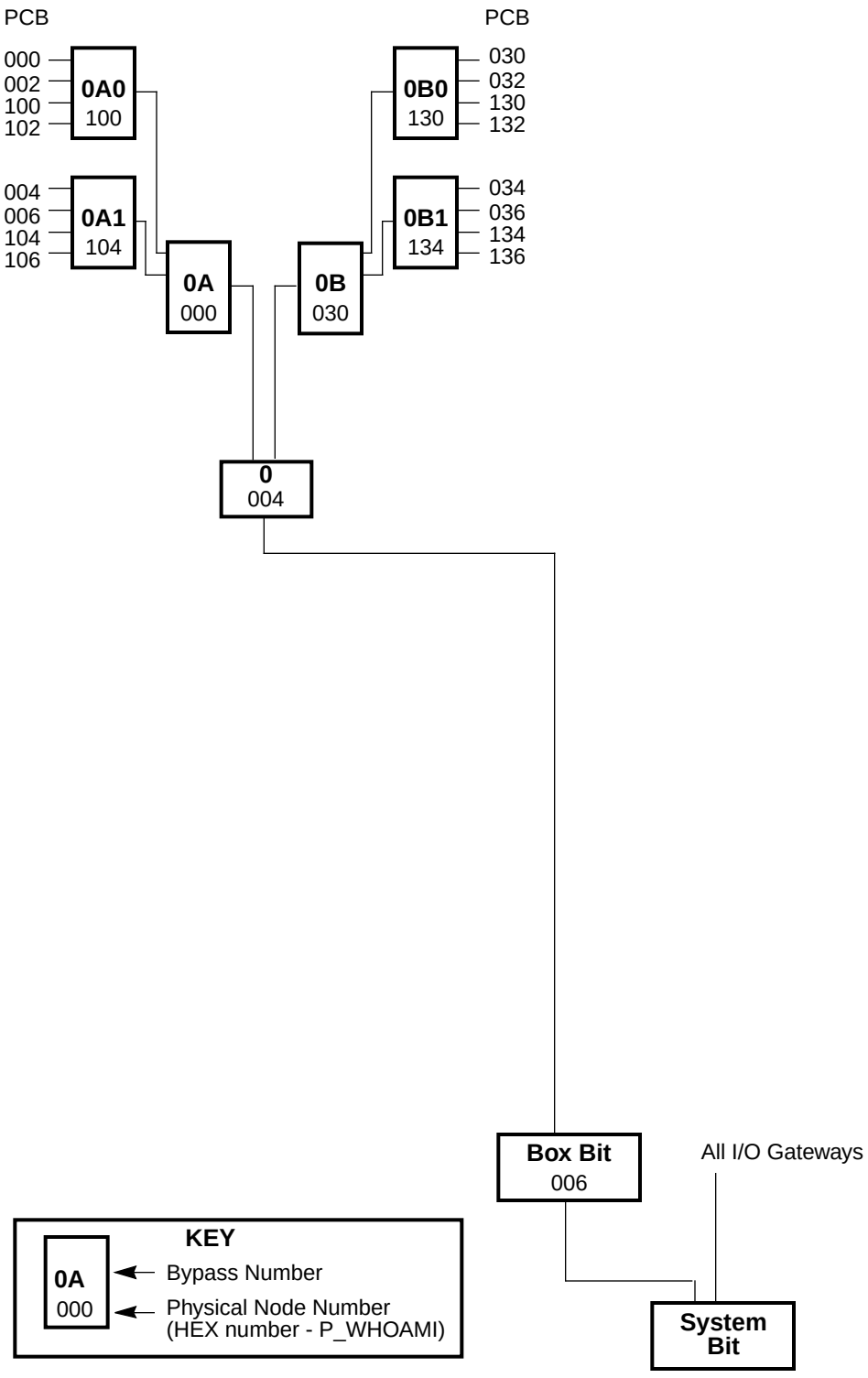
The PCB bypass points are controlled by bit 2^{11} or bit 2^{12} of the network mode register (NODE_CSR). Every processing element node PCB contains four PCB bypass points (one for each physical barrier synchronization circuit).

Each PCB bypass point is given a name that corresponds to the physical node that controls the bypass point. For example, the PCB bypass point 002 in barrier synchronization circuit 0 is located on the PCB that contains physical PEs 002_{16}, 003_{16}, 012_{16}, and 013_{16}. This bypass is controlled by setting bit 2^{11} of the NODE_CSR in physical node 002 (which contains physical PEs 002_{16} and 003_{16}) to the appropriate value.

When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 0, the output of the AND gate in a PCB bypass point is redirected to the fanout block in the bypass point. When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 1, the output of the AND gate in a PCB bypass point is directed to a second-level bypass point.

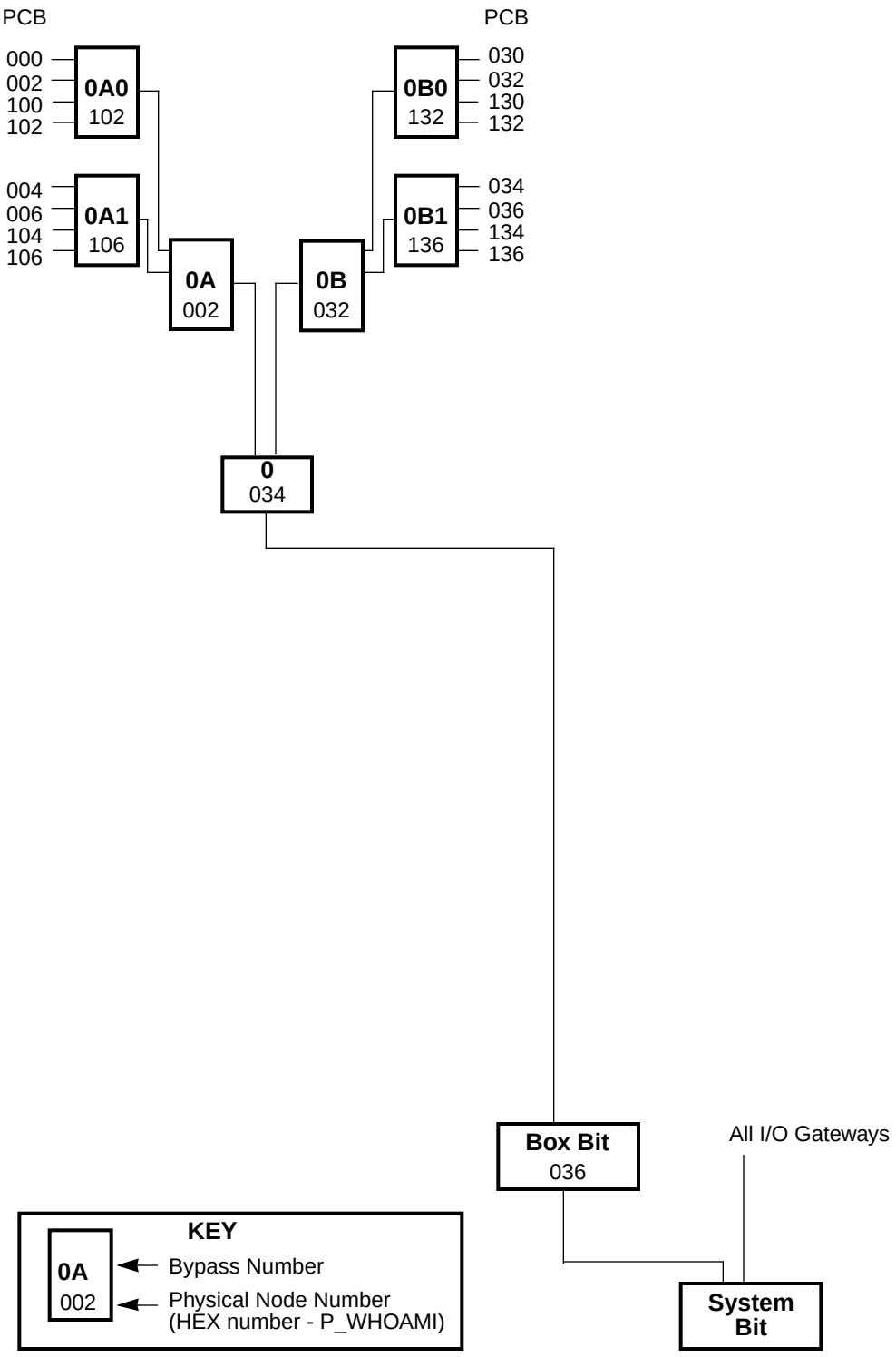
The other bypass points shown in the following figures are controlled by bit 2^{13} of the NODE_CSR. For example, bypass point 0A in barrier synchronization circuit 0 of cabinet 0 is controlled by setting bit 2^{13} of the NODE_CSR in physical node 000_{16} (which contains physical PEs 000_{16} and 001_{16}) to the appropriate value.

When bit 2^{13} of the NODE_CSR is set to 0, the output of the AND gate in the bypass point is redirected to the fanout block in the bypass point. When bit 2^{13} of the NODE_CSR is set to 1, the output of the AND gate in the bypass point is directed to the next-level bypass point.



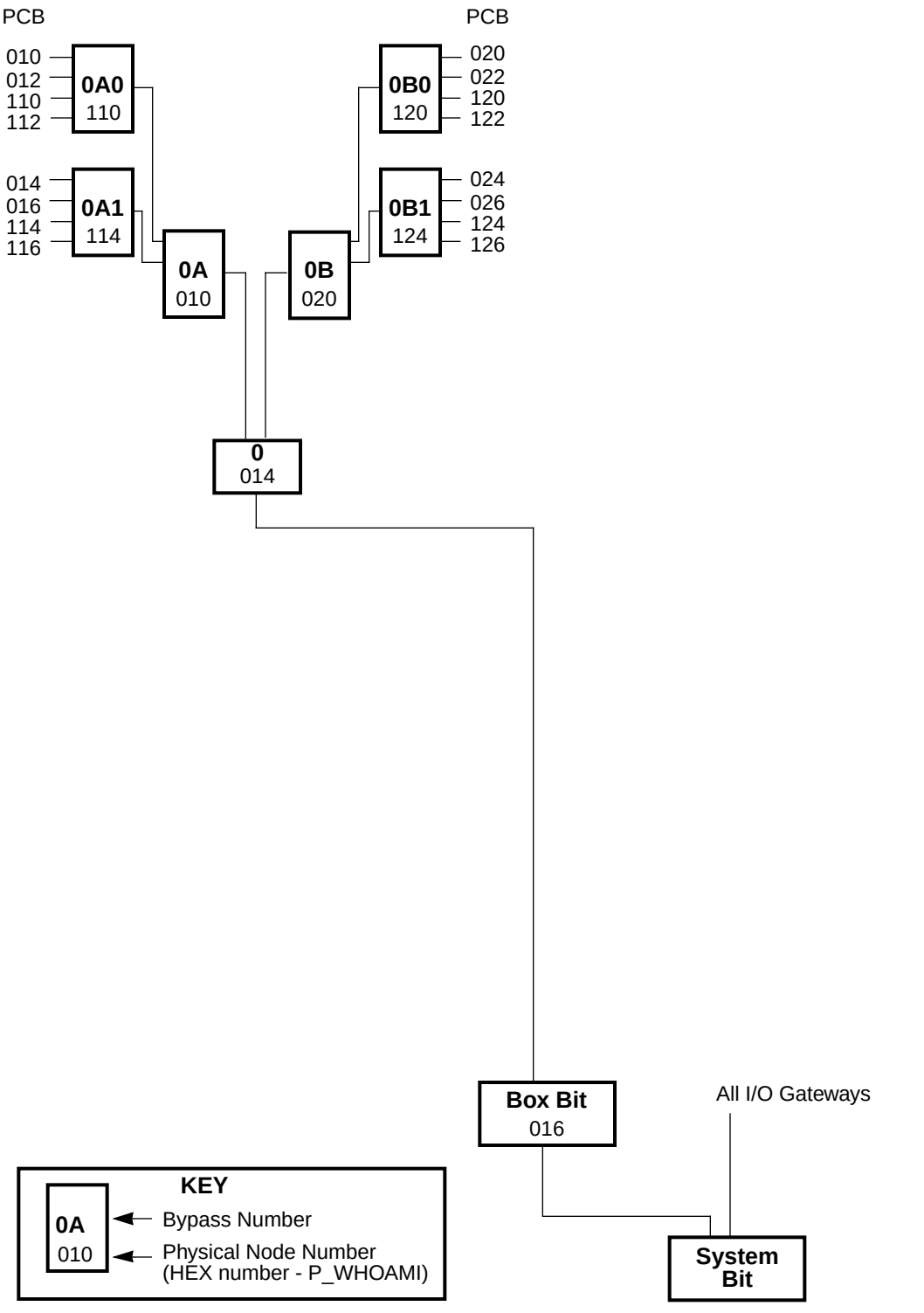
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 83. Barrier Synchronization Circuit 0 in CRAY T3D MC64 System



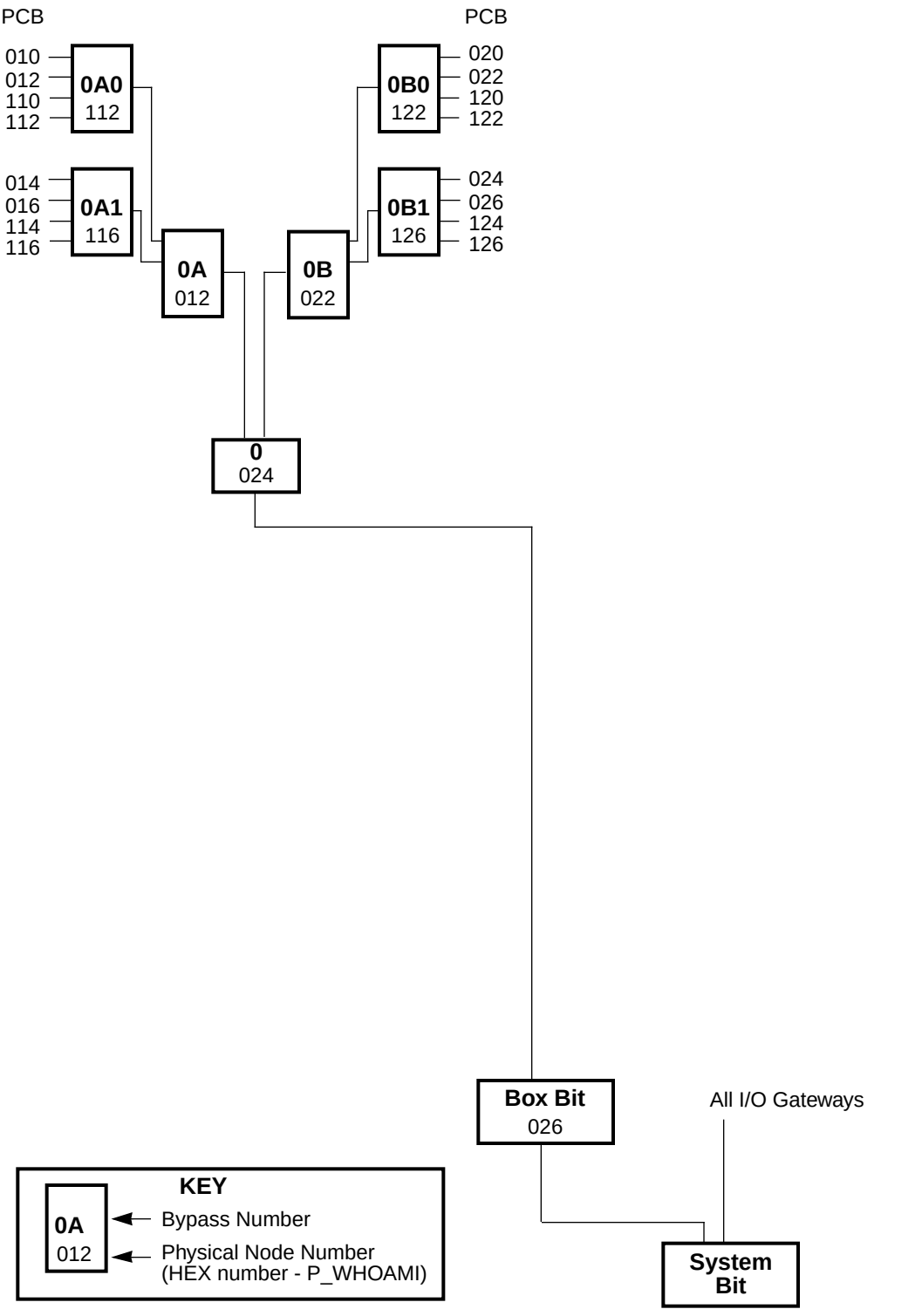
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 84. Barrier Synchronization Circuit 1 in CRAY T3D MC64 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 85. Barrier Synchronization Circuit 2 in CRAY T3D MC64 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 86. Barrier Synchronization Circuit 3 in CRAY T3D MC64 System

8 CRAY T3D MC32 System

The CRAY T3D MC32 system contains 32 PEs in 16 processing element nodes and is housed in one cabinet. The CRAY T3D MC32 system is only used in system test and check out (STCO).

The following subsections describe the communication links, module layout, and barrier synchronization bypass points for the CRAY T3D MC32 system.

NOTE: Throughout this document, physical PE numbers are represented as three-digit hexadecimal numbers that correspond to the physical PE numbers in the P_WHOAMI registers. For example, a PE may have a physical PE number of $10B_{16}$.

NOTE: Throughout this document, physical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a P_WHOAMI register with bit 2^0 set to 0. For example, physical node $10A_{16}$ contains the physical PEs $10A_{16}$ and $10B_{16}$.

NOTE: Throughout this document, logical node numbers are represented as three-digit hexadecimal numbers. This number is equivalent to the number read from a L_WHOAMI register with bit 2^0 set to 0. For example, logical node $10A_{16}$ contains the logical PEs $10A_{16}$ and $10B_{16}$.

8.1 CRAY T3D MC32 Communication Links

Figure 87 shows the physical communication links between nodes in the Y dimension.

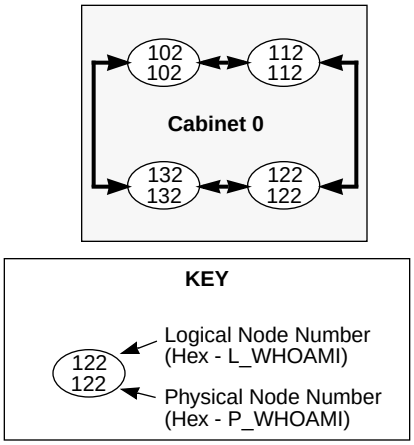


Figure 87. CRAY T3D MC32 Y-dimension Communication Links

Figure 88 shows the physical communication links between the nodes in the X and Z dimensions. For clarity the figure does not show the communication links that complete the torus in the X and Z dimensions.

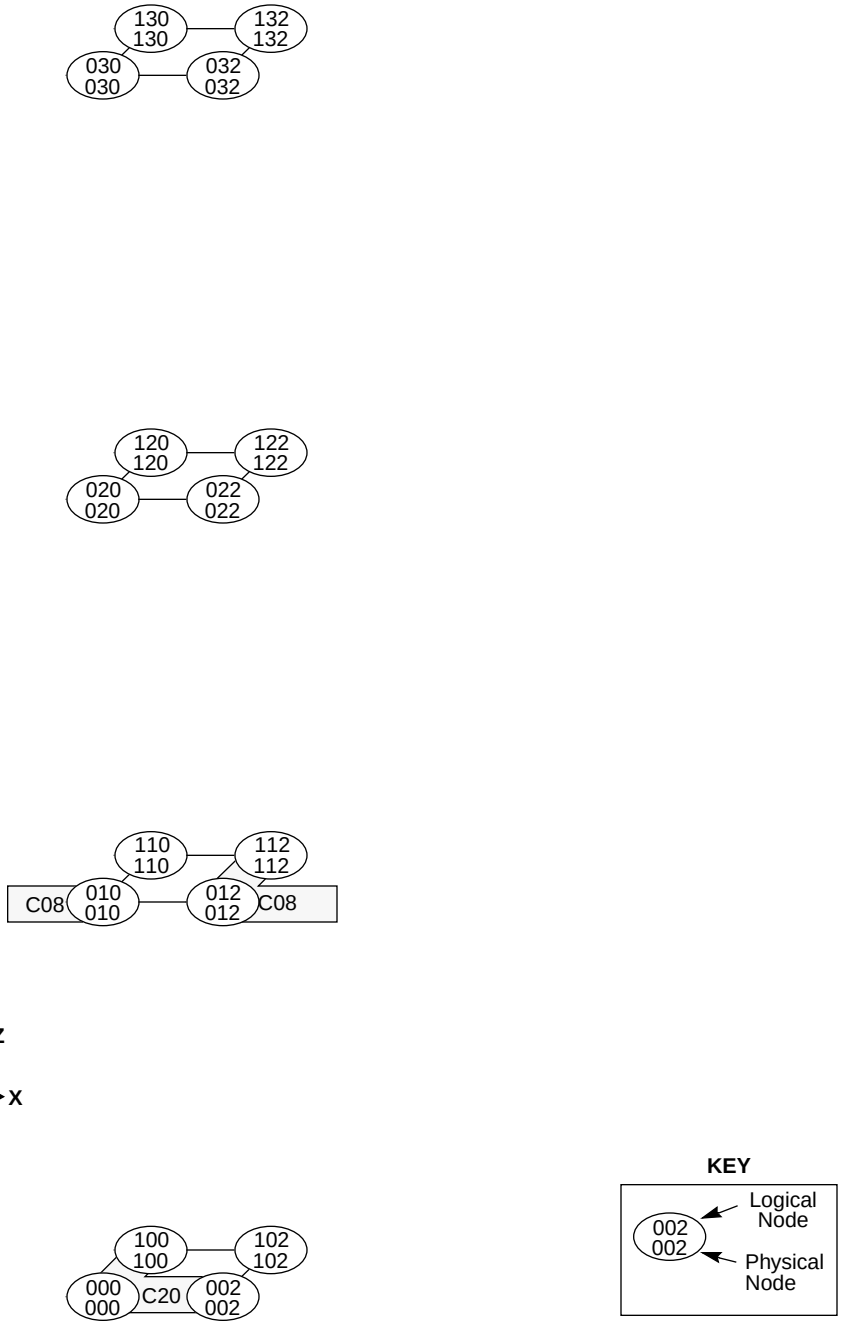


Figure 88. CRAY T3D MC32 X- and Z-dimension Communication Links

NOTE: The I/O gateway C08 does not connect to the same nodes in a CRAY T3D MC32 system as it does in a CRAY T3D MC128 system.

8.2 CRAY T3D MC32 Module Layout

Figure 89 shows the module layout and physical node locations in the CRAY T3D MC32 system cabinet. Each figure represents the physical node number as a three-digit hexadecimal number that is equivalent to the number read from the P_WHOAMI register with bit 2^0 set to 0. For example, physical node 002_{16} contains the physical PEs 002_{16} and 003_{16}.

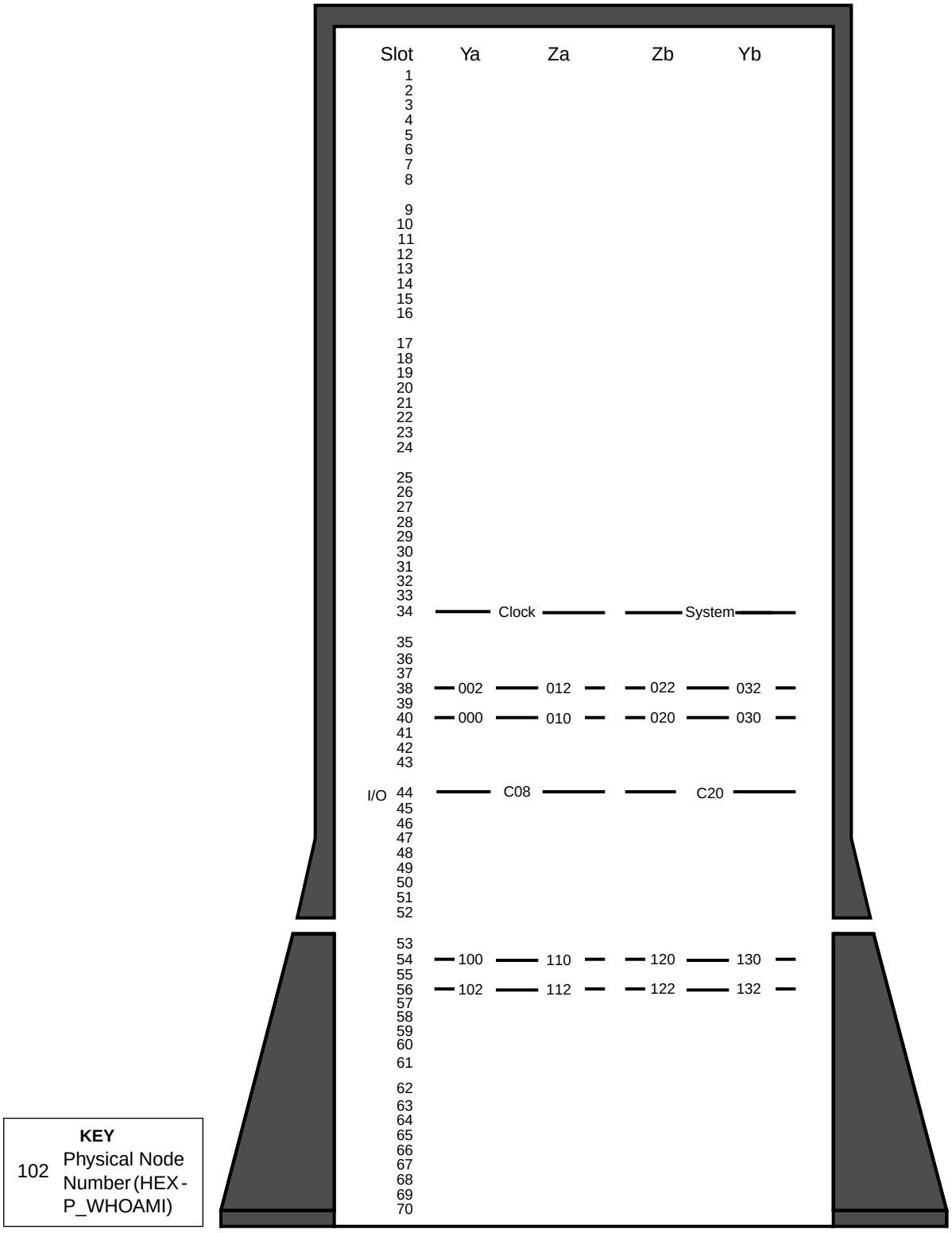


Figure 89. CRAY T3D MC32 Module Layout

8.3 CRAY T3D MC32 Barrier Synchronization Circuits

Figure 90 through Figure 93 show the barrier synchronization bypass points for all four physical barrier synchronization circuits in the CRAY T3D MC32 system. In these figures, the printed circuit board (PCB) bypass points and all other bypass points are shown.

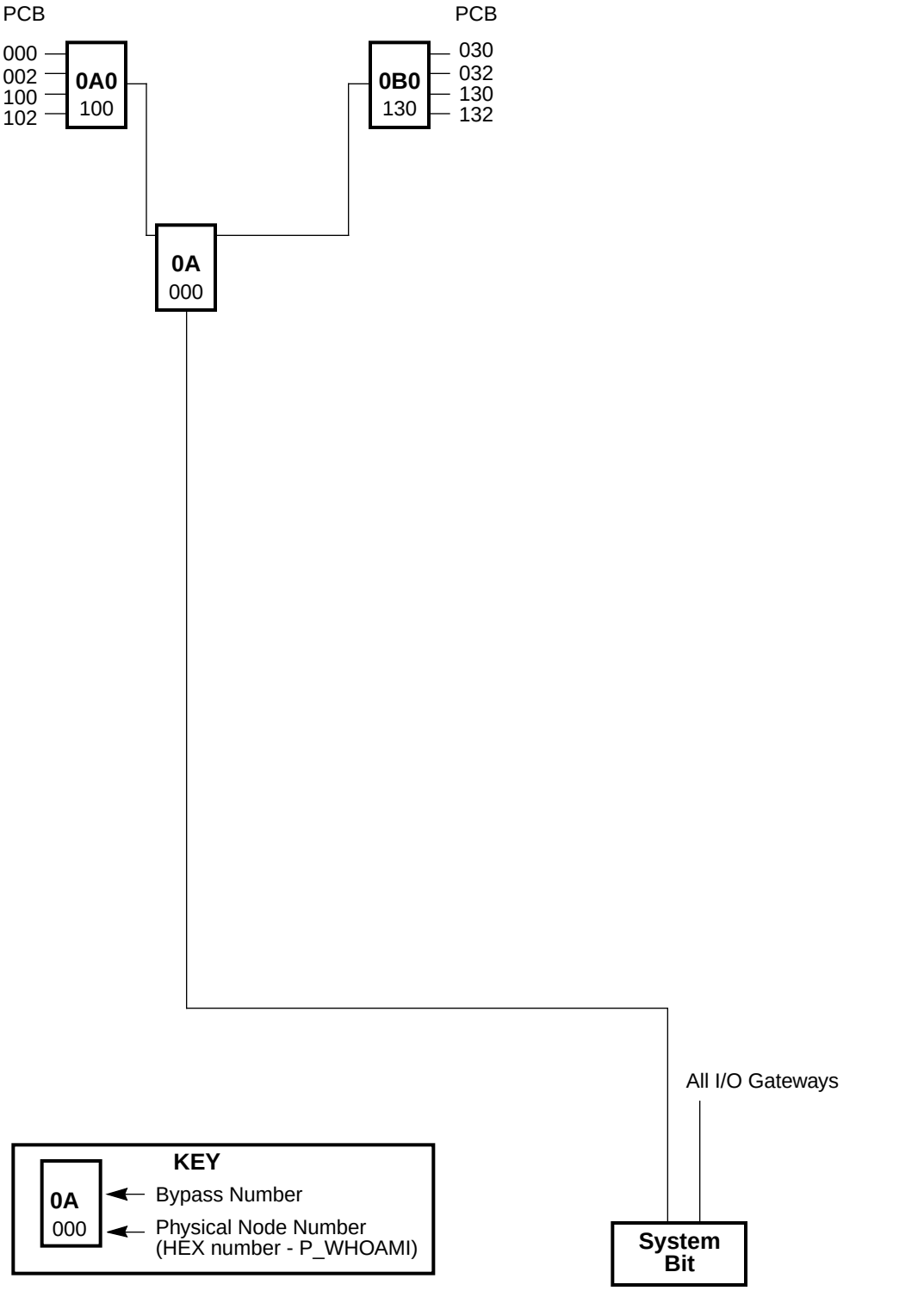
The PCB bypass points are controlled by bit 2^{11} or bit 2^{12} of the network mode register (NODE_CSR). Every processing element node PCB contains four PCB bypass points (one for each physical barrier synchronization circuit).

Each PCB bypass point is given a name that corresponds to the physical node that controls the bypass point. For example, the PCB bypass point 402 in barrier synchronization circuit 0 is located on the PCB that contains physical PEs 402_{16}, 403_{16}, 412_{16}, and 413_{16}. This bypass is controlled by setting bit 2^{11} of the NODE_CSR in physical node 402 (which contains physical PEs 402_{16} and 403_{16}) to the appropriate value.

When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 0, the output of the AND gate in a PCB bypass point is redirected to the fanout block in the bypass point. When bit 2^{11} or bit 2^{12} of the NODE_CSR is set to 1, the output of the AND gate in a PCB bypass point is directed to a second-level bypass point.

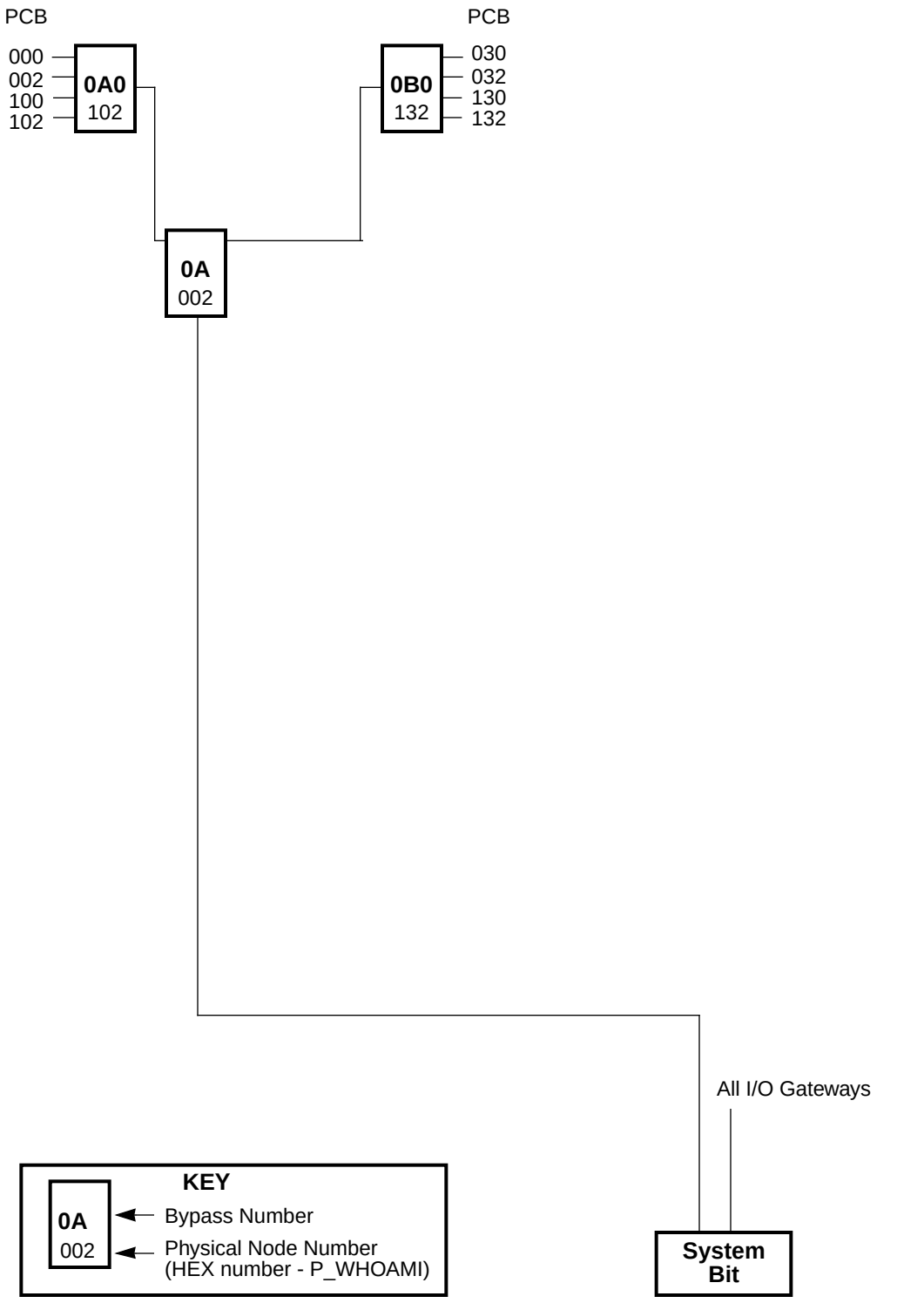
The other bypass points shown in the following figures are controlled by bit 2^{13} of the NODE_CSR. For example, bypass point 0A in barrier synchronization circuit 0 of cabinet 0 is controlled by setting bit 2^{13} of the NODE_CSR in physical node 000_{16} (which contains physical PEs 000_{16} and 001_{16}) to the appropriate value.

When bit 2^{13} of the NODE_CSR is set to 0, the output of the AND gate in the bypass point is redirected to the fanout block in the bypass point. When bit 2^{13} of the NODE_CSR is set to 1, the output of the AND gate in the bypass point is directed to the next-level bypass point.



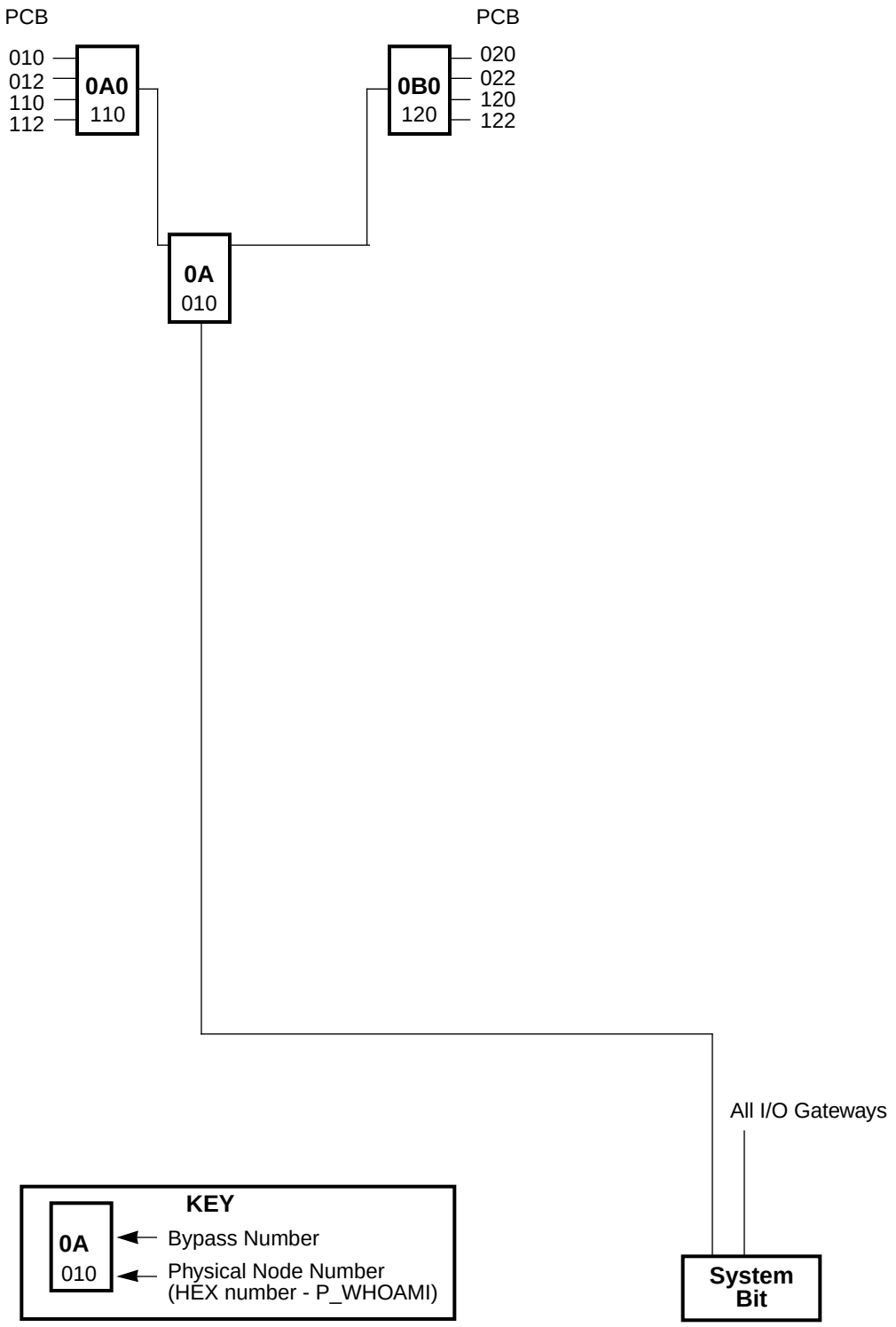
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 90. Barrier Synchronization Circuit 0 in CRAY T3D MC32 System



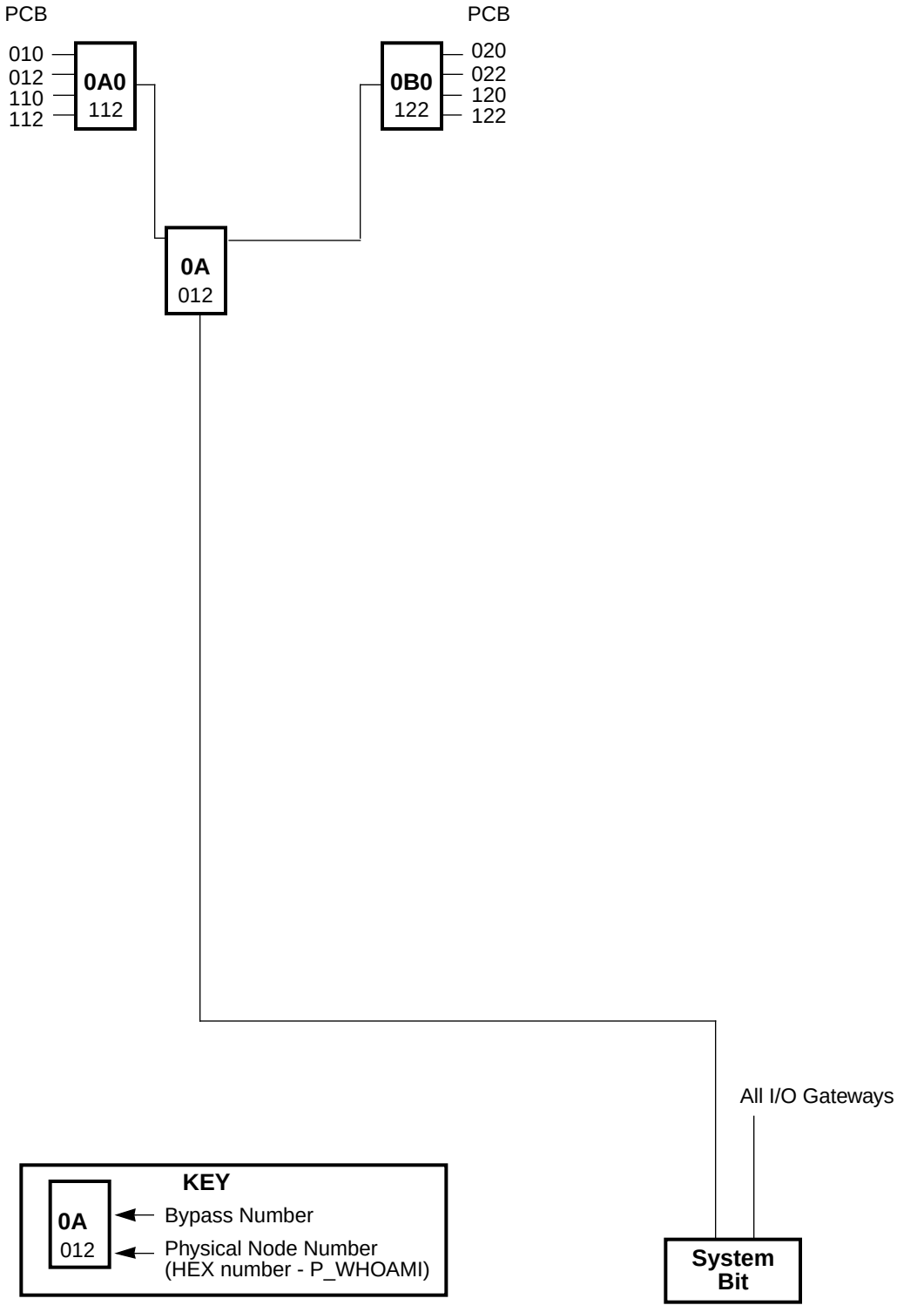
NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 91. Barrier Synchronization Circuit 1 in CRAY T3D MC32 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{11} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 92. Barrier Synchronization Circuit 2 in CRAY T3D MC32 System



NOTE: The PCB bypass points shown in this figure are controlled by bit 2^{12} of the NODE_CSR. The other bypass points shown in this figure are controlled by bit 2^{13} of the NODE_CSR.

Figure 93. Barrier Synchronization Circuit 3 in CRAY T3D MC32 System